Compute-In-Memory with SAR ADC & 2T1C DRAM for MAC Operations

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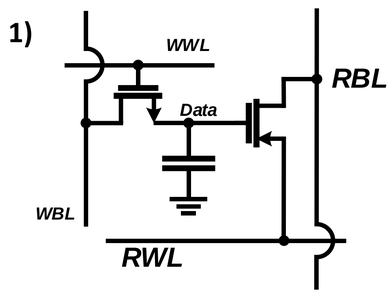
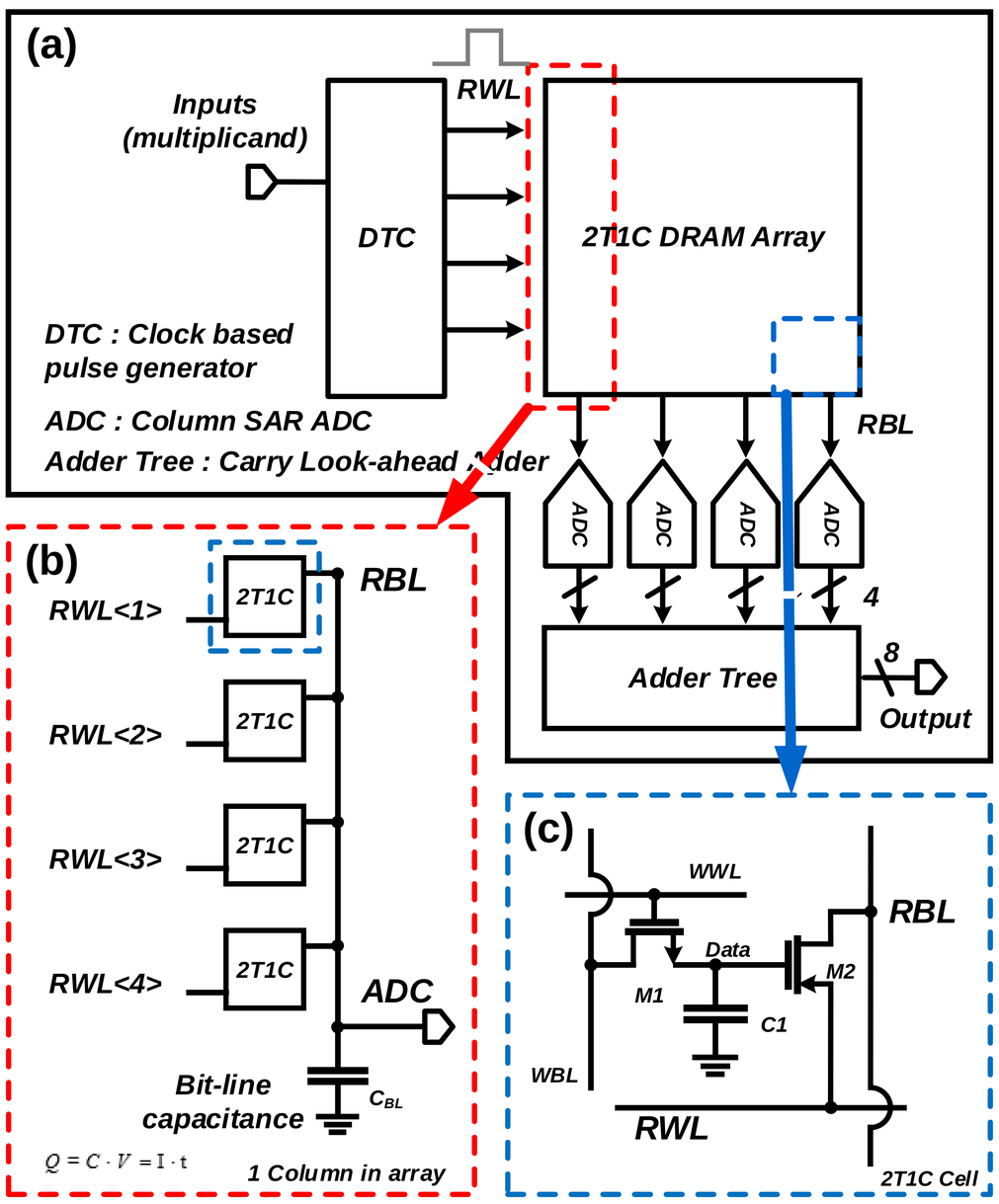
Introduction



1) : 2T1C DRAM cell using NMOS as access MOS, and PMOS as readout MOS

- In 2T1C DRAM, data can be read non-destructive through read-word-line (RWL) & read-bit-line (RBL).
- Since the format of data is current of readout MOS, charge is stacked in RBL as time goes.
- We proposed multiplication & summation in memory using particular time pulse to RWL, and saturation current of readout MOS in saturation condition.

Proposed CIM Circuit & System



a) **Overall structure of CIM** – DTC unit converts input bits into clock-based pulse width signal, signal goes through read-word-line of 2T1C cell. After charge stacking, using ADC to get column calculation data.

b) **1 Read-bit-line column schematic in array** – Input signal goes through readout MOS(M2), current came out depends on cell data, and stacking charge at bit-line capacitance in parallel.

c) **2T1C DRAM cell**

▪ Read-Bit-Line Charge Stacking Operation

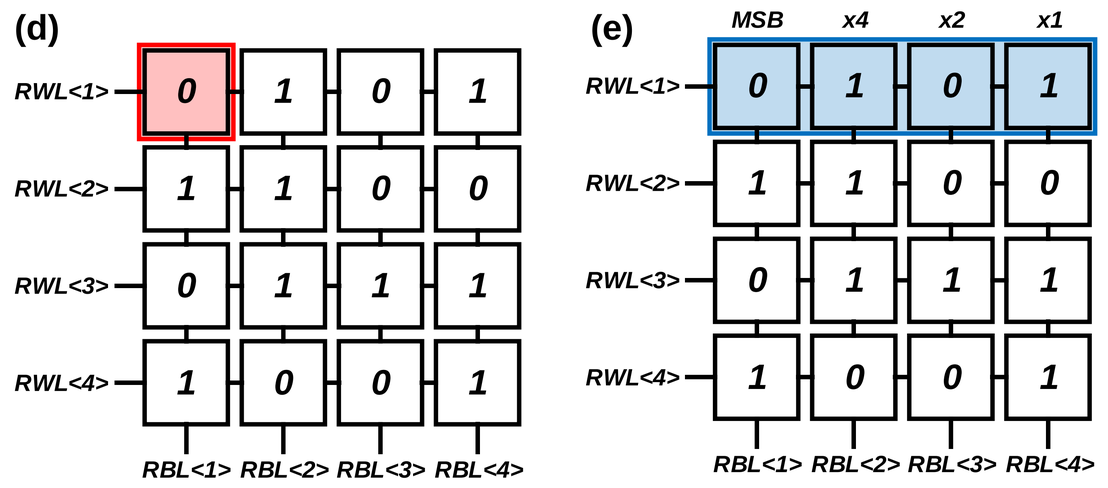
* : PMOS readout → data 0 = VDD, data 1 = GND

- Charge stacks depends on cell data.

2) **Cell data<1~4>** is 1 → all turned on

3) **Cell data<1&4>** is 1 → only cell 1, 4 is turned on

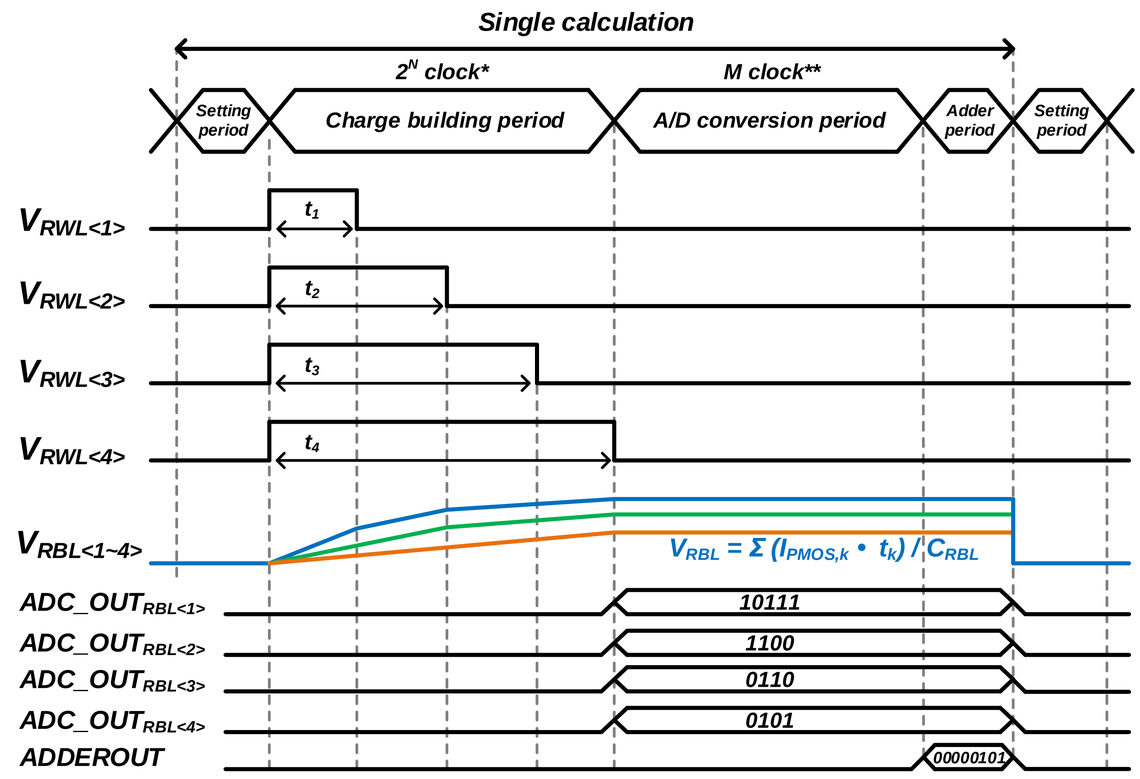
Additional Bit-line Digit Weight



(d) : Calculation is proceeds in column parallel. Therefore, cell data can be only 1-bit (0 & 1).
(e) : To achieve multi-bit cell data, Weigh the digits in each column from (x1) to (MSB).

- Multiplication & summation is done in each RBL.
- Results in each column contains additional digit weight data.
- Using digital adder tree to finish digit calculation at final step of total operation as shown in diagram **(a)**.

Simulation Results

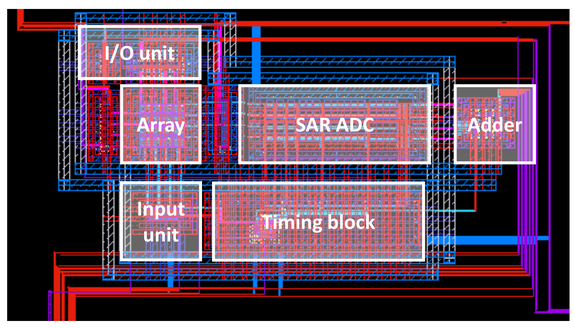


* : N = # of input bit, ** : M = # of ADC bit

- As pulse width of RWL signals are different, and so are the data in cells, amount of stacked charge in column is different.
- Using SAR ADC to convert each V_{RBL} into digital code (***ADC_OUT***), then adder tree finishes digit calculation (***ADDEROUT***).

Chip Layout and Summary *(Test in progress)*

▪ Full Chip Layout



Process Tech.	1poly-7metal 28nm CMOS
Memory Size	16-bit
Bit Cell Area	10um x 10um (100um^2)
# of Input	2-bit x4
# of Weight	4-bit x4
Output	8-bit x1
Chip Size	400um x 200um (0.08mm^2)
Power Domain	1 V (Digital)
System CLK Frequency	100MHz
MAC Calculation Time	14 clock
SAR ADC Resolution	4-bit
Power Consumption	7.2 μW/single multiplication