An Ultra Low-power Low-offset Double-tail Comparator

Ata Khorami[a], Roghayeh Saeidi[b], Mohammad Sharifkhani[a], Nima Taherinejad[c]
[a] Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran.
[b] Telecommunication Research Center (ITRC), Tehran, Iran.
[c] Institute for Computer Technology (ICT), TU Wien, Vienna, Austria.

***Abstract*— In double tail comparators, the pre-amplifier amplifies the input differential voltage and when the output V_{cm} of the pre-amplifier becomes larger than V_{th} of the latch input transistors, the latch is activated and finalizes the comparison. As a result, the pre-amplification delay is fixed to a value and cannot be set at the minimum required delay, to save power and improve offset. In fact, when the latch is activated the pre-amplifier output differential voltage is still growing but the latch finishes the comparison before the maximum differential gain is formed and applied to the latch. In this paper, a comparator is proposed in which the pre-amplifier is turned *off* when the maximum gain is achieved so that always the maximum possible gain is applied to the latch. Therefore, not only the input referred offset is improved but also the power consumption of the pre-amplifier is saved. Simulations in 0.18µm technology show with an appropriate pre-amplification delay the average power is saved by up to 75% while the offset voltage is reduced by about 30%.**

Keywords—double tail comparator; low-offset comparator; low-power comparator; appropriate pre-amplification delay;

I. INTRODUCTION

Dynamic comparators are essential parts of different mixed-mode circuits specially ADCs [1, 2]. They are being used in several portable/wearable electronic devices and sensor node applications [3]. Therefore, the power and speed of the comparators considerably affect the total performance of the system [4, 5]. Single tail comparator is one of the first dynamic comparators reported [6]. In this structure, the pre-amplifier amplifies the input differential voltage ($V_{in+}-V_{in-}=V_{id}$) while the latch is amplifying the result to *Vdd* and *Vss*. In single tail comparators, the rail-to-rail output swing of the pre-amplfier (which is merged with the latch in one stage) is leaked to the inputs of the comparator through gate-drain capacitors. The leaked voltage to the inputs of the pre-amplifier is called kickback noise [7]. Single-tail comparators suffers from a large kickback noise which is not tolerable in applications where capacitors are at the input of the pre-amplifier (holding a value) such as capacitive DACs in SAR ADCs [8, 9]. That's why later, double-tail comparators where introduced [10-14]. In double-tail comparators, the pre-amplifier stage is a separated stage followed by a latch stage, therefore, a very small fraction of the large output swing of the latch is leaked to the inputs of the pre-amplifier. That's because the kickback noise is propagated to the pre-amplifier inputs through a series connection of the gate-drain capacitors of the latch (which is small) and the pre-amplifier input transistors. When employing double tail comparators become regular in mixed-mode designs, several researches have been done to improve their power, offset, and speed. The following presents some of the recently proposed methods to improve the offset voltage and power consumption of the double tail comparators.

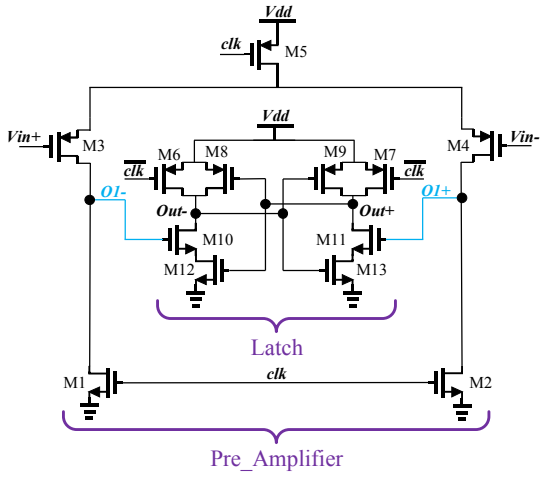
In [13], a bulk tuned calibration technique is used to reduce the offset voltage, so the size of the input transistors to achieve a lower power consumption. However, the calibration routines reduces the speed and adds up more complexity and a considerable area to the circuit. The area is mostly coming from the calibration capacitors. A double-tail comparator is proposed in [14] which employs a half latch in the pre-amplifier. This method efficiently reduces the power consumption but it increases the kickback noise due to the large swing of the cross-coupled circuit in the pre-amplifier. In [15], a double tail comparator with a low kickback noise is introduced, however, this comparator increases the power consumption or reduces the speed, since the pre-amplifier is always kept *on*. The comparator proposed in [16] uses a simple latch whose output nodes are connected to the output nodes of the pre-amplifier. This comparator reduces the power, although it suffers from kickback noise. Also, for high resolution applications (low offset voltage) the power efficiency reduces, since the latch must fully charge and discharge the large output parasitic capacitors of the pre-amplifier. In [17], it has been shown that the power consumption of the dynamic comparators can be reduced by limiting the output voltage swing of the pre-amplifier. Using this method, the power is reduced but for a considerable power reduction another supply voltage is required which sinks current. This will add complexity and power to the circuit. The methods reported in [1, 10, 11, 18] reduce the power consumption and increase the speed by a wise management of the pre-amplification process, however, they are not able to reduce the offset voltage. In [2], a low-offset comparator is proposed for low-voltage applications, however, the offset voltage is still large compared to a conventional comparator at nominal *Vdd*. This comparator is an efficient candidate for low-voltage applications. The comparator presented in [19] enhanced the offset and power, however, it reduces the speed because of its special structure. In fact, during pre-amplification, the output common-mode voltage of the pre-amplifier is growing turning off the input PMOS transistors of the latch. As one of the most recent works, the comparator reported in [20] reduces the power consumption using a forward body biased scheme. This method is successful in power reduction for ultra-low-voltage low-speed applications. Moreover, the comparator presented in [3] reduces the power consumption and enhances the speed but it increases the kickback noise due to its special pre-amplfier.

In this paper a comparator is proposed which is able to reduce the power consumption and offset voltage considerably. First, the conventional and proposed double-tail comparators are introduced; then, the benefits of the proposed structure are discussed and simulation results are

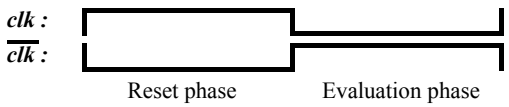
presented. A comparison shows that the proposed comparator is able to reduce the power consumption by up to 75%.

II. The Double-Tail Comparator

Fig. 1 presents a common version of double-tail comparators [10, 13, 21]. This comparator is comprised of a pre-amplifier circuit followed by a latch circuit.



(a)



(b)

Fig. 1. (a,b) The circuit and control signals of the conventional comparator.

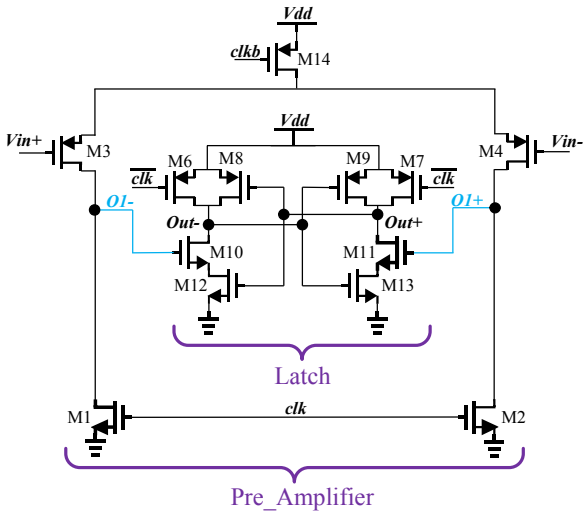
In the reset phase, *clk* ="1", $\overline{clk}$ ="0", therefore, the pre-amplifier outputs (O1-,O1+) are discharged to *Gnd* and the latch outputs (Out-, Out+) are charged to *Vdd*. To trigger the evaluation phase *clk* and $\overline{clk}$ are changed to *clk*="0", $\overline{clk}$ ="1"; Then, the output capacitors of the pre-amplifier are charged differentially. Gradually, a differential voltage, V_{diff}, appears at the pre-amplifier outputs. When the common mode voltage of the pre-amplifier output parasitic capacitors (V_{cmp}) become larger than the voltage threshold of the latch input transistors (M10, M11), V_{th}, the latch is turned *on* and finalizes the comparison.

In the conventional comparator, during the evaluation phase, the pre-amplifier increases the differential gain until the pre-amplifier input transistors go to the triode region. After that, the differential gain is reduced approaching zero as the pre-amplifier output nodes go to *Vdd*. When the latch is activated and finishes the comparison, a small V_{diff} is available at its inputs. If at the moment that a large V_{diff} is available at the outputs of the pre-amplifier, the pre-amplifier is turned *off* not only the power is saved but also during the whole latching process the maximum V_{diff} is applied to the latch reducing the offset voltage. Moreover, the latch operates stronger (with a higher input V_{diff}) reducing the short circuit power of the latch.

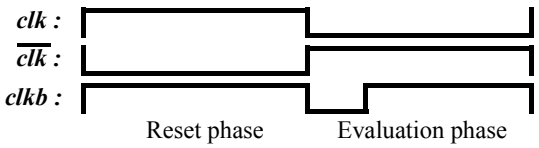
III. The Proposed Comparator

Fig. 2 presents the proposed comparator. In this comparator, during the reset phase, the outputs of the pre-amplifier and the latch are discharged to *Vss* and charged to *Vdd*, respectively. In the evaluation phase, the pre-amplifier creates a differential voltage at its output; when the gain goes to its maximum value, the pre-amplifier is turned *off* and the latch finishes the comparison.

In the proposed structure, when the maximum gain is achieved, the pre-amplifier is turned *off* to save the power of the pre-amplifier. Moreover, the maximum differential gain will remain at the outputs of the pre-amplifier applying to the latch until the end of the comparison. Therefore, the effect of the latch on the input referred offset voltage is minimized.



(a)



(b)

Fig. 2. The circuit and the control signals of the proposed comparator.

As disscussed earlier, the pre-amplifier increases the differential gain until the input transistors go to the triode region. The delay from the beginnig of the evaluation phase to the moment of maximum differential gain depends on the current of M3 and M4 so the input V_{cm} of the comparator. The more the V_{cm} the higher the delay, and the lower the V_{cm} the lower the delay will be. Therefore, the control circuit should turn *off* the pre-amplifier based on the value of input V_{cm} of the compator; in order to create such a delay, a delay line-based controller can be designed such as the one proposed in [3]. The V_{cm} of input signals should affect the delay of one of the gates in the controller so that V_{cm} can change the pulsewidth of the controller output (pre-amplification delay in Fig. 2(b)).

As discussed earlier, in the control circuit, if the input voltages of the comparator (V_{in+}, V_{in-}) are high the pre-amplification delay (the width of *clkb*) increases, and if the

input voltages of the comparator are low the pre-amplification delay reduces. Therefore, the pulse width of *clkb* is proportional to the input V_{cm} of the comparator. This is exactly what is required considering the variation in the delay of the maximum gain moment (when the maximum gain is achieved).

IV. Simulation Results

In order to make a clear comparison, the proposed and conventional comparators were designed for the same clock frequency of *1GHz* using 0.18*μm* CMOS technology. In fact, first the conventional comparator was designed; then, the proposed method is applied to the conventional circuit keeping the sizing of the transistors the same. Then the control circuit was designed to create the appropriate delay which is about 80 *ps* and 220 *ps* for lowest and highest input V_{cm}. It is noteworthy that the power consumption of the control circuit is less than 9% of the total power consumption of the proposed comparator which is negligible. Also, the area of the controller is lower than 3% of the total area. Generally, the controller presented in [3] adds few overhead to the circuit, however, it is very effective in power and offset reduction.

Fig. 3 presents the power consumption of the proposed comparator versus the comparator of Fig. 1. As, seen, the proposed comparator reduces the power consumption significantly. The average power consumption is reduced by 65%. Around V_{cm}=0V, the power is reduced by about 75%.

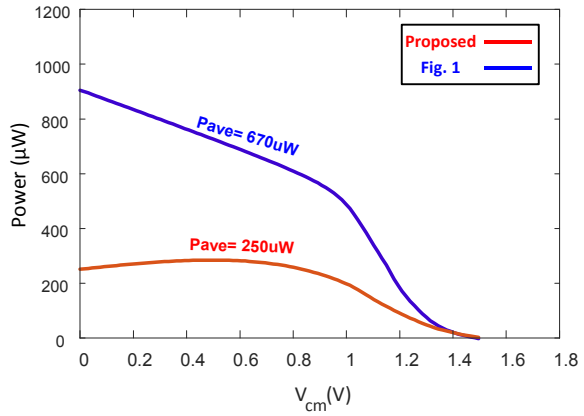


Fig. 3. Power consumption of the proposed and conventional comparators at 1GHz clock frequency.

Fig. 4 presents the offset voltage versus the input V_{cm} of the comparator. The proposed method reduces the offset voltage by about 20%-30% in the whole V_{cm} range.

The delay of the comparators is depicted in Fig. 5. The delay of both comparators are comparable, however, the power consumption of the proposed comparator is considerably lower.

Table 1 presents a comparison between the proposed and some previously reported comparators. The proposed comparator is able to work at high frequencies while it conumes very low power. The proposed comparator is a good choice for high-speed low-power applications.

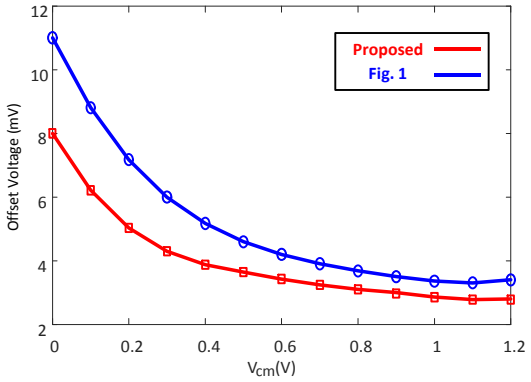


Fig. 4. Offset votlage of the proposed and cenventioanl

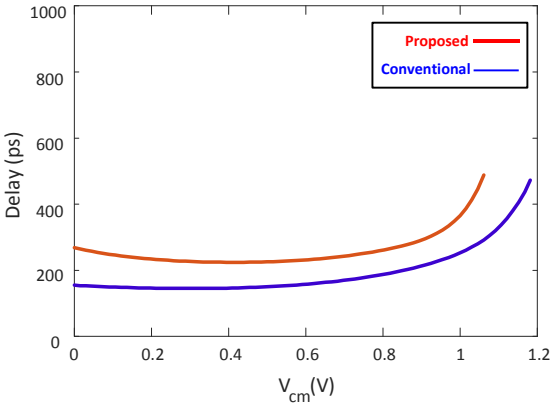


Fig. 5. Delay versus input V_{cm} of the comparators at V_{id} =10mV.

TABLE I. A COMPARISON BETWEEN THE PROPOSED AND SOME OTHER COMPARATORS

	[1]	[2]	[3]	Fig.1	**This**
Supply (V)	1.2	1.2	1.8	1.8	1.8
Freq (GHz)	1.25	0.5	0.5	1	1
Power avg (*μW*)	600	18.6	230	675	250
σ_{off} (mV), Vcm=0.5Vdd	7.78	36.5	2	2.8	3.5
Technology	130nm	180nm	180nm	180nm	180nm

V. Conclusion

A low-power low offset double-tail comparator is presented. In this comparator, the pre-amplification delay is manipulated in a way to minimize the power consumption and the offset voltage. The area, and speed overhead of the proposed comparator is negligible. Simulations in 0.18μm CMOS technology prove the low-power behavior of the proposed comparator. This comparator reduces the power consumption by up to 75%. Also, the input referred offset voltage is reduced due to a higher differential gain applied to the latch.

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