

Device Variability Analysis for Memristive Material Implication

Simon Michael Laube and Nima TaheriNejad

Abstract—Currently, memristor devices suffer from variability between devices and from cycle to cycle. In this work, we study the impact of device variations on memristive Material Implication (IMPLY). New constraints for different parameters and variables are analytically derived and compared to extensive simulation results, covering single gate and 1T1R crossbar structures. We show that a static analysis based on switching conditions is not sufficient for an overall assessment of robustness against device variability. Furthermore, we outline parameter ranges within which the IMPLY gate is predicted to produce correct output values. Our study shows that threshold voltage is the most critical parameter. This work helps scientists and engineers to understand the pitfalls of designing reliable IMPLY-based calculation units better and design them with more ease. Moreover, these analyses can be used to determine whether a certain memristor technology is suitable for implementation of IMPLY-based circuits and systems.

Index Terms—Memristor, ReRAM, Material Implication, IMPLY, Logic, In-Memory Computation, Variation, Robustness, Analytical Studies, Simulations.

I. INTRODUCTION

Memristors are used for memory applications [1]–[5], where even storage of multiple bits per device is feasible [6]–[9]. In addition, memristors have become increasingly popular for neural network and learning applications [10], [11], by exploiting their analog, synapses-like nature. Another application of memristors is implementing digital (in-memory) logic [12]–[14], such as IMPLY, for various computations [15]–[20]. At the moment these applications – more often than not – are not verified by physical implementation and experimental data [21]. This imbalance leads to many problems when actual physical implementation is desired. While material sciences have certainly progressed in this field [22]–[24], the circuit-level interface to higher abstraction levels is not yet ready to provide a reliable base for proposed applications [21]. Some of the fundamental problems, that need to be considered at design time, are inter-device variability and cyclic variability. In larger structures, usually implemented within crossbar arrays, sneak paths and wire resistance are an even bigger issue [25], [26]. While the two latter have received an acceptable level of attention from the community, the two former have been less explored and addressed by the community. We hope that this work encourages and provides pointers to the community to move in that direction.

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Here, we aim to provide a better insight into the operation of a single memristive IMPLY logic gate by considering device variations. Similar works on that topic already exist, such as [27]–[29], which mainly focus on other types of memristor-based logic. The most relevant work to ours is [29], where the focus is set on the design of the IMPLY circuit itself, and an alternative operation “NOT IMPLY (NIMP)” is proposed to mitigate certain problems. In contrast, our work explores regular IMPLY in more detail, particularly regarding the effect of device variations on the IMPLY operation, and leaves the NIMP approach for future works. We note that there is a variety of memristors based on different physical effects [22]. From the perspective of this work, the internal mechanism is to a large extent inconsequential. Hence, we use the general term, memristor, to refer to *resistive switching elements* or Resistive Random Access Memorys (ReRAMs) and, when needed, specify what may make the internal mechanisms important. The main contribution of this work to the field of memristor-based logic, is an in-depth mathematical analysis of memristive IMPLY regarding its constraints due to device variation. Plausibility of the proposed constraints is verified via simulations using a popular model.

The rest of this paper is organized as follows: Section II, particularly Section II-A, reviews memristive IMPLY logic and shows its limitations. An introduction to the crossbar architecture is given in Section II-B and the device model is described in Section III. In Section IV, we formulate new constraints for the IMPLY gate, before comparing them to the single gate simulation results in Section V. The results of the crossbar simulations are presented in Section VI and compared against the single gate simulation and constraints. We conclude the paper in Section VII.

II. MATERIAL IMPLICATION (IMPLY)

The truth table of IMPLY, and its four different cases, are shown in Table I. It takes two input states p and q and outputs q' . Not every type of memristor is suitable for material implication. The devices have to exhibit *voltage threshold behavior*. Moreover, all devices used for an operation shall have the same parameter values (resistance range, threshold voltages, switching speed).

A. Gate structure and constraints

Two memristors and a resistor are necessary for a single memristive IMPLY gate. Figure 1(b) shows such a gate, with abstracted drivers and sense circuitry. Each memristor can be *set* (forced to Low Resistance State (LRS)) by applying a

Table I
TRUTH TABLE OF MATERIAL IMPLICATION AND ITS FOUR CASES

Cases	p	q	q'
Case 1	0	0	1
Case 2	0	1	1
Case 3	1	0	0
Case 4	1	1	1

voltage $|V_{\text{set}}| > |v_{\text{on}}|$ with appropriate (in our case *negative*) polarity; and can be *reset* (forced to High Resistance State (HRS)) by applying $|V_{\text{reset}}| > |v_{\text{off}}|$ with an opposite polarity¹. If a memristor is set, it represents logic state ‘1’; if it is reset, it represents logic state ‘0’ [12]. During initialization, these voltage amplitudes are applied to each device, while the other is kept floating. For the actual logic operation both devices are driven at the same time: V_{cond} is applied to node R and V_{set} to node T of Figure 1(b). For a correct operation

$$|V_{\text{set}}| > |v_{\text{on}}| \quad (1)$$

$$|V_{\text{set}} - V_{\text{cond}}| < |v_{\text{on}}| \quad (2)$$

$$|V_{\text{reset}}| > |v_{\text{off}}| \quad (3)$$

must hold. Moreover, the circuit designer needs to select a valid value for R_G , as described in [30].

It is important to note that only in Case 1 of Table I the output memristor Q is actually changing its state. However, during this process the voltage across each device changes too. It is valid to ask if this has an effect on the result of the operation, and the answer is yes. Using Kirchhoff’s circuit laws (KCL), Chen et al. [29] showed that there are two possible final steady states of the operation:

- 1) The normalized state variable s reaches the upper boundary of 1 ($R_Q = R_{\text{on}}$) before the voltage across Q falls below the threshold v_{on} . The final steady state is $R_Q = R_{\text{on}}$.
- 2) V_Q falls below the threshold v_{on} before s reaches 1. In this case the steady state resistance can be expressed as²:

$$R_{\text{min}} = \frac{-v_{\text{on}} R_G R_{\text{off}}}{(R_G + R_{\text{off}})(V_{\text{set}} + v_{\text{on}}) - R_G V_{\text{cond}}} \quad (4)$$

¹This is true for bipolar switching mechanisms. Phase Change (PC) based devices, for example, may use the same voltage polarity for set and reset.

²Note that in our convention $v_{\text{on}} < 0$.

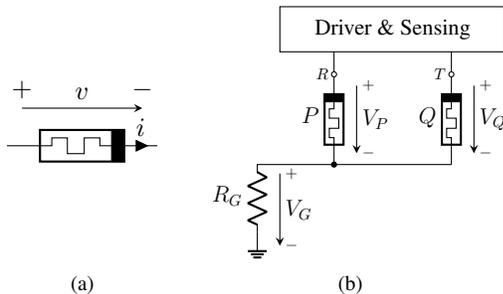


Figure 1. (a) Memristor symbol and defined voltage polarity used in this work. (b) A single IMPLY gate.

An important point to mention is that this calculation is based on the premise, that the driving voltages of P and Q are chosen such that there is *no state drift* in P during operation.

B. Crossbar principles

Crossbar architectures are a natural candidate for memristor-based logic, as high integration density can be reached. In so called 1R (or 1M) crossbars, a memristor device is fabricated at each intersection of bit- and word-lines, which act as the access medium for the cell. 1R crossbars are very difficult to handle [31]–[33], even if parasitics are not considered. Many works have been carried out to study effects [25], [34]–[36], or solve them [14], [26], [34], but thus far 1T1R has been the preferred implementation [31]–[33]. 1T1R (or 1T1M) crossbars, consist of a transistor and a memristor in each cell. The transistor in each cell cost extra area but they prevent the cells from switching state when a cell is not part of an operation (not selected). One possible, readout scheme is provided by [26], which we use in this work. The chosen readout scheme [26] provides a closed-form solution. Moreover, it introduces very little additional complexity, which enables this work to remain focused on issues regarding IMPLY itself. In Section VI we compare crossbar simulation results against single gate results and outline the differences.

III. DEVICE MODEL

There are a range of different simulation models for memristors [37]–[40]. For the simulations presented in this paper, the TU Wien LTSpice implementation [21], [41] of VTEAM [38] was used. An overview of the model is given in Equations (5) to (9), with a memristor polarity as shown in Figure 1(a).

In VTEAM, w acts as the state variable and represents a length between the extrema w_{on} and w_{off} ($w \in [w_{\text{off}}, w_{\text{on}}]$). Here, we define the relation of these state variable boundaries

$$w_{\text{on}} > w_{\text{off}} \quad (5)$$

and define the normalized state variable ($s \in [0, 1]$):

$$s(w) = w' = \frac{w - w_{\text{off}}}{w_{\text{on}} - w_{\text{off}}} \quad (6)$$

These definitions may be changed, as long as the model equations are updated, too. The rate of change of the state variable, w , is defined by

$$\frac{dw}{dt} = \begin{cases} k_{\text{off}} \left(\frac{v}{v_{\text{off}}} - 1 \right)^{\alpha_{\text{off}}} f_{\text{off}}(w) & 0 < v_{\text{off}} < v \\ 0 & v_{\text{on}} < v < v_{\text{off}} \\ k_{\text{on}} \left(\frac{v}{v_{\text{on}}} - 1 \right)^{\alpha_{\text{on}}} f_{\text{on}}(w) & v < v_{\text{on}} < 0 \end{cases} \quad (7)$$

which is the essential building block of the model [38]. In this equation k_{on} , k_{off} , v_{on} , v_{off} , α_{on} and α_{off} represent fitting parameters, while $f_{\text{on}}(w)$ as well as $f_{\text{off}}(w)$ are window functions that limit dw/dt .

I/V -characteristics and window functions are not defined in the model and thus can be freely chosen. We chose a linear current/voltage dependency:

$$R(w) = R_{\text{off}} + (R_{\text{on}} - R_{\text{off}}) \cdot s(w) \quad (8)$$

By rearranging the equation we can further express $s(R)$ for any (measured) R :

$$s(R) = \frac{R - R_{\text{off}}}{R_{\text{on}} - R_{\text{off}}} \quad (9)$$

The same expressions as for the Simmon's Tunnel Barrier model in [37] were chosen as window functions. In addition, w is bounded and thus cannot exceed w_{on} or w_{off} .

The studies presented in this paper are kept as general as possible, however, simulations need model parameters. Rather than introducing arbitrary parameter values, we experimentally fitted [18] our VTEAM model to Known BS-AF-W [42] memristors we had at the time. Parameters shown in Table III, represent a best effort fitting we conducted previously [18].

IV. FORMULATING CONSTRAINTS

This section marks the beginning of our new contributions. In this section, we mathematically extract device variability constraints which govern and limit operations of IMPLY. At first, we define the notation: Each parameter involved in the analysis is written as $\xi_{i,M}$, where $\xi \in \{R, v, k\}$, $M \in \{P, Q\}$ and $i \in \{\text{off}, \text{on}\}$. For example, the off-resistance of memristor P in this notation would be denoted as $R_{\text{off},P}$.

Logic thresholds determine the logic state of a device. They are defined separately for input (I) and output (O), as well as logic '1' (H) and '0' (L). Indices are used to denote the respective logic thresholds, e.g. R_{IL} is the input threshold for logic '0'.

A. Static behavior

Each case in the truth table (Table I) imposes constraints onto the voltage V_Q across memristor Q , as certain *switching conditions* must be met. They can be analyzed via KCL and represent a *static* view of the circuit. The constraints can be used to find limits for $R_{\text{on},P}$, $R_{\text{off},P}$, $v_{\text{on},Q}$ and $v_{\text{off},Q}$. They do not provide limits for $R_{\text{on},Q}$ or $R_{\text{off},Q}$, as R_Q in this context is the target output resistance state that Q must reach during IMPLY. Therefore, R_Q is later set according to the chosen output logic threshold: $R_Q \leq R_{\text{OH}}$ or $R_Q \geq R_{\text{OL}}$. Applying KCL in Figure 1(b) gives us the voltage across Q as

$$V_Q = \frac{R_Q(R_P + R_G)V_{\text{set}} - R_Q R_G V_{\text{cond}}}{R_P R_G + R_P R_Q + R_Q R_G}. \quad (10)$$

First we solve Equation (10) with a generalized threshold voltage, v , and the solution is specialized for each case afterwards. The first switching condition is:

$$V_Q > v. \quad (11)$$

Plugging Equation (10) into Equation (11) and isolating R_P leads to

$$R_P \cdot b > a, \quad (12)$$

where

$$a = R_Q R_G (v + V_{\text{cond}} - V_{\text{set}}), \quad (13)$$

$$b = R_Q V_{\text{set}} - v(R_G + R_Q). \quad (14)$$

At this point the relation in 12, is divided by b . Therefore, depending on the value of b , we have

$$\begin{cases} R_P > \frac{a}{b} & \text{if } b > 0 \\ R_P < \frac{a}{b} & \text{if } b < 0 \\ R_P \rightarrow \pm\infty & \text{if } b = 0 \end{cases} \quad (15)$$

Next, the switching condition

$$V_Q < v \quad (16)$$

is examined. Following the same steps as before, we have

$$\begin{cases} R_P < \frac{a}{b} & \text{if } b > 0 \\ R_P > \frac{a}{b} & \text{if } b < 0 \\ R_P \rightarrow \pm\infty & \text{if } b = 0 \end{cases} \quad (17)$$

Since the third case ($b = 0$) in Equations (15) and (17) yields³ $\pm\infty$, it is of no interest for the rest of the analysis. The first two cases in Equations (15) and (17) both provide limits for v and R_P , respectively.

Here, the resulting equations (constraints) are specialized for each of the four cases of the truth table using the respective switching conditions. R_Q is set to the associated output logic threshold (R_{OH} or R_{OL}). Only the first case ($b > 0$) of Equations (15) and (17) is considered, since the second case ($b < 0$) only provides negative limits, and $R_P > 0$. For every case of the truth table, according to our notations, $v_{\text{on}} < 0$ and $v_{\text{off}} > 0$. Hence, we have

Case 1 $V_Q > -v_{\text{on},Q}$

$$v_{\text{on},Q} > -V_{\text{set}} \frac{R_{\text{OH}}}{R_G + R_{\text{OH}}} \quad (18)$$

$$R_{\text{off},P} > \frac{R_{\text{OH}} R_G (V_{\text{cond}} - v_{\text{on},Q} - V_{\text{set}})}{R_{\text{OH}} V_{\text{set}} + v_{\text{on},Q} (R_G + R_{\text{OH}})} \quad (19)$$

Case 3: $V_Q < -v_{\text{on},Q}$

$$v_{\text{on},Q} > -V_{\text{set}} \frac{R_{\text{OL}}}{R_G + R_{\text{OL}}} \quad (20)$$

$$R_{\text{on},P} < \frac{R_{\text{OL}} R_G (V_{\text{cond}} - v_{\text{on},Q} - V_{\text{set}})}{R_{\text{OL}} V_{\text{set}} + v_{\text{on},Q} (R_G + R_{\text{OL}})} \quad (21)$$

Case 2/Case 4: $V_Q > -v_{\text{off},Q}$

$$v_{\text{off},Q} > -V_{\text{set}} \frac{R_{\text{OH}}}{R_G + R_{\text{OH}}} \quad (22)$$

$$R_{\text{off},P} > \frac{R_{\text{OH}} R_G (V_{\text{cond}} - v_{\text{off},Q} - V_{\text{set}})}{R_{\text{OH}} V_{\text{set}} + v_{\text{off},Q} (R_G + R_{\text{OH}})} \quad (23)$$

$$R_{\text{on},P} > \frac{R_{\text{OH}} R_G (V_{\text{cond}} - v_{\text{off},Q} - V_{\text{set}})}{R_{\text{OH}} V_{\text{set}} + v_{\text{off},Q} (R_G + R_{\text{OH}})} \quad (24)$$

Equations (18), (20) and (22) directly result from $b > 0$, whereas Equations (19), (21), (23) and (24) are the respective relations derived from $R_P > a/b$ in Equation (15) and $R_P < a/b$ in Equation (17).

³That is, as long as $|a|$ is neither zero, nor ∞ .

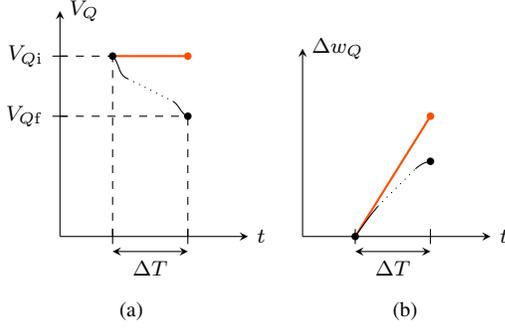


Figure 2. A symbolic voltage-time curve for V_Q (a) an induced state change Δw_Q (b) during a single IMPLY operation of duration ΔT . The estimations for the formulation of constraints are drawn in orange, the symbolic representations of the actual curves in black.

Some additional static constraints are given by the choice of logic thresholds. That is,

$$R_{\text{off},P} > R_{\text{IL}} \quad (25)$$

$$R_{\text{off},Q} > R_{\text{IL}} \quad (26)$$

$$R_{\text{on},P} < R_{\text{IH}} \quad (27)$$

$$R_{\text{on},Q} < R_{\text{IH}}. \quad (28)$$

Similar to standard logic families, input and output thresholds may differ. From the point-of-view of these constraints, only input thresholds need to be considered, as they determine whether or not the device states fed to the operation are valid in the first place.

B. Dynamic behavior

With respect to the static analysis, the chosen timestep of operation can introduce much stricter constraints. For exact solutions, one would have to solve the differential state equation of the chosen model (in our case Equation (7) from VTEAM). This is not a trivial task and might not even be possible for all models. Thus, in this section we derive a lower boundary for $v_{\text{on},Q}$, but not the infimum, which cannot be exceeded by the exact (or numeric) solution. That way we take into account the state change (dynamic behavior) of memristors during the operation, using an acceptable estimation. We note that in doing such an analysis, the chosen model is assumed to be accurate. However, in practice no existing model represents all the reality and physics involved.

The main idea of our estimation is to look at how V_Q changes over time in Case 1 of the truth table, while assuming negligible state drift in P . As R_Q changes from HRS to LRS, V_Q decreases. Thus, the initial voltage V_{Qi} is the highest occurring value of V_Q during that timestep, while the final voltage V_{Qf} is the lowest – symbolically shown in Figure 2(a). If the device characteristics are such that the highest V_Q corresponds to the maximum value of dw/dt – in our case true due to Equation (7) – a hard limit can be expressed. KCL can be used to describe the initial voltage

$$V_{Qi} = \frac{R_{\text{off},Q}(R_{\text{off},P} + R_G)V_{\text{set}} - R_{\text{off},Q}R_G V_{\text{cond}}}{R_{\text{off},P}R_G + R_{\text{off},P}R_{\text{off},Q} + R_{\text{off},Q}R_G}. \quad (29)$$

Plugging V_{Qi} into Equation (7) gives the initial rate of state change⁴:

$$\left. \frac{dw_Q}{dt} \right|_{\text{initial}} = \frac{\Delta w_Q}{\Delta T} = k_{\text{on},Q} \left(\frac{-V_{Qi}}{v_{\text{on},Q}} - 1 \right)^\alpha \quad (30)$$

Now we set the actual dw_Q/dt equal to the initial rate for the whole timestep ΔT . Through this simplification a maximum Δw_Q for the given timestep ΔT can be found, which cannot be exceeded:

$$\Delta w_Q = k_{\text{on},Q} \left(\frac{-V_{Qi}}{v_{\text{on},Q}} - 1 \right)^\alpha \Delta T \quad (31)$$

This is because the estimation provides a better overall situation towards the correct operation result, when compared to the actual situation. That is, as we see in Figure 2(b), the estimated Δw_Q is always larger than the actual value. To obtain a correct result after the IMPLY operation, R_Q must at least reach the logic threshold R_{OH} . Otherwise the result would not be interpreted as logic ‘1’. Via Equation (9) we can find $s(R_{\text{OH}})$. In combination with Equation (6), the necessary Δw_{min} can be expressed as

$$\Delta w_{\text{min}} = \frac{R_{\text{OH}} - R_{\text{off},Q}}{R_{\text{on},Q} - R_{\text{off},Q}} (w_{\text{on}} - w_{\text{off}}) + w_{\text{off}}, \quad (32)$$

and

$$\Delta w_Q \geq \Delta w_{\text{min}} \quad (33)$$

shall be true. Plugging the previous terms into Equation (33) gives

$$v_{\text{on},Q} \geq \frac{-V_{Qi}}{\alpha \sqrt{\frac{\Delta w_{\text{min}}}{k_{\text{on},Q} \Delta T}} + 1}, \quad (34)$$

which is the newly found constraint. As this relation contains multiple parameters of P and Q apart from $v_{\text{on},Q}$, it provides boundaries for all of them. For example, a certain $v_{\text{on},Q}$ restricts $R_{\text{off},P}$ to a specific range, and in turn a certain $R_{\text{off},P}$ restricts $v_{\text{on},Q}$ to a specific range.

Considering Equation (34), a question is whether the same estimation could be used to find an upper limit for $v_{\text{on},Q}$. Such an analysis, however, is not meaningful for memristor Q . Both, a minimum value of dw/dt and a maximum value Δw_{max} , must be specified. The later does not exist for Q since a high w_Q (ideally w_{on}) is desired in Case 1.

There is, however, a Δw_{max} for memristor P , as a change of R_P is generally not desired. By definition the logic state of P remains unchanged if $R_P > R_{\text{IL}}$. Only if this is true, it can be used as an input for an operation. As R_P drifts away from $R_{\text{off},P}$ (ideal HRS), V_P decreases. Thus, the minimum value of dw/dt is the *final value* at the end of the operation, in contrast to V_{Qi} being the initial value. The final value V_{Pf} cannot be expressed easily, as R_{Pf} and R_{Qf} are unknown. Hence, another simplification must be made: We evaluate V_{Pf} using $R_P = R_{\text{off},P}$, as if there was no state drift in the first place:

$$V_{Pf,j} = \frac{R_{\text{off},P}(R_{Q,j} + R_G)V_{\text{cond}} - R_{\text{off},P}R_G V_{\text{set}}}{R_{\text{off},P}R_G + R_{\text{off},P}R_{Q,j} + R_{Q,j}R_G} \quad (35)$$

⁴ f_{on} is missing in Equation (30) because $f_{\text{on}} \approx 1$ for $w_Q < w_{\text{on}}$

Due to this very rough estimation, we expect the constraint to represent a fairly weak boundary. Therefore,

$$R_{Q,1} = R_{\min,Q} \quad (36)$$

$$R_{Q,2} = \frac{R_{\text{off},Q} + R_{\min,Q}}{2} \quad (37)$$

$$R_{Q,3} = \sqrt{R_{\text{off},Q} \cdot R_{\min,Q}} \quad (38)$$

are used to evaluate V_{P_f} in Equation (35) and obtain a range within which the circuit is less likely to fail. The first value, Equation (36), is the theoretical minimum for $R_{\text{on},Q}$, which is the ideal R_{Q_f} . However, the actual $R_{Q,f}$ can take on any value between $R_{\text{off},Q}$ and $R_{\min,Q}$. Hence, in a second estimation, Equation (37), we assume that R_{Q_f} is the arithmetic mean of $R_{\text{off},Q}$ and $R_{\min,Q}$. In other words, the final state is halfway between the initial state and the ideal endstate ($R_{\min,Q}$). However, if V_{P_f} is plotted over R_Q on a linear scale, it reveals that the dependence is non-linear. Thus, $R_{Q,2}$ might not be the best estimation either. The dependence is, nevertheless, approximately linear on a semi-logarithmic scale; so our third estimation, Equation (38), assumes R_{Q_f} to be the geometric mean of $R_{\text{off},Q}$ and $R_{\min,Q}$. If the timestep of IMPLY operation is limited, we do not expect $R_{Q,1}$ to provide an appropriate estimation, since this is the overall optimum scenario. $R_{Q,2}$ and $R_{Q,3}$ might both be of value to the circuit designer, because they represent a non-ideal scenario, chosen based on design parameters.

Following the same steps as before, we can formulate the constraint for $v_{\text{on},P}$:

$$\Delta w_P = k_{\text{on},P} \left(\frac{-V_{P_f,j}}{v_{\text{on},P}} - 1 \right)^\alpha \Delta T \quad (39)$$

$$\Delta w_P \leq \Delta w_{\text{max}} \quad (40)$$

$$v_{\text{on},P} \leq \frac{-V_{P_f,j}}{\alpha \sqrt{\frac{\Delta w_{\text{max}}}{k_{\text{on},P} \Delta T}} + 1} \quad (41)$$

Table II provides a summary of relevant constraints on memristor parameters, that were derived in this section. Most of these relations depend on multiple parameters of both memristors. Thus, the permissible value range of one parameter is impacted by the values of other parameters, and vice versa. Once the value of a parameter is determined (either decided by the designer or given by the technology) respective equations in Table II determine the tolerable range of variation in others. This bidirectional view enables us to define an operating area, which, in turn, allows us to predict how the circuit will react to variations in the concerned parameters.

V. SIMULATION – SINGLE GATE

A. Circuit design

The simulated circuit corresponds to the circuit shown in Figure 1(b), with the addition that R_G can be shorted by a parallel switch. The driver circuits are ideal voltage sources with serial switches for High-Z mode. Each switch is modeled with an on-resistance of $1 \text{ n}\Omega$ and an off-resistance of $1 \text{ G}\Omega$. Given the memristor properties, especially R_{on} and R_{off} , five circuit-level parameters have to be determined. These are $R_G, V_{\text{set}}, V_{\text{cond}}, V_{\text{reset}}$ and V_{read} . Choosing V_{reset} is somewhat

Table II
SUMMARY OF RELATED CONSTRAINTS ON PARAMETERS OF P AND Q .

Constraint	Constrained parameters
$v_{\text{on},Q} > f(R_Q \equiv R_{\text{OH}})$ Equation (18)	$v_{\text{on},Q}$
$R_{\text{off},P} > f(v_{\text{on},Q}, R_Q \equiv R_{\text{OH}})$ Equation (19)	$R_{\text{off},P}, v_{\text{on},Q}$
$v_{\text{on},Q} > f(R_Q \equiv R_{\text{OL}})$ Equation (20)	$v_{\text{on},Q}$
$R_{\text{on},P} < f(v_{\text{on},Q}, R_Q \equiv R_{\text{OL}})$ Equation (21)	$R_{\text{on},P}, v_{\text{off},Q}$
$v_{\text{on},Q} > f(R_{\text{off},P}, R_{\text{on},Q}, R_{\text{off},Q}, k_{\text{on},Q})$ Equation (34)	$R_{\text{off},P}, R_{\text{on},Q}, R_{\text{off},Q}, v_{\text{on},Q}, k_{\text{on},Q}$
$v_{\text{on},P} < f(R_{\text{on},P}, R_{\text{off},P}, R_{\text{off},Q}, k_{\text{on},P})$ Equation (41)	$R_{\text{on},P}, R_{\text{off},P}, R_{\text{off},Q}, v_{\text{on},P}, k_{\text{on},P}$
$R_{\text{on},P} < R_{\text{IH}}$, Equation (27)	$R_{\text{on},P}$
$R_{\text{off},P} > R_{\text{IL}}$, Equation (25)	$R_{\text{off},P}$
$R_{\text{on},Q} < R_{\text{IH}}$, Equation (28)	$R_{\text{on},Q}$
$R_{\text{off},Q} > R_{\text{IL}}$, Equation (26)	$R_{\text{off},Q}$

Table III
NOMINAL VALUES OF MODEL AND CIRCUIT PARAMETERS.

Parameter Value	v_{on} −0.7 V	v_{off} 10 mV	R_{on} 10 k Ω	R_{off} 1 M Ω	k_{on} 1 cm/s	
Parameter Value	α_{on} 3	α_{off} 3	w_{on} 3 nm	w_{off} 0 nm	k_{off} −0.5 nm/s	
Parameter Value	a_{on} 3 nm	a_{off} 0 nm	w_c 0.1 nm			
Parameter Value	V_{set} 1.0 V	V_{cond} 0.9 V	V_{reset} −1.0 V	V_{read} 0.1 V	R_G 40 k Ω	T 15 μs

straightforward, as it is only used for initialization and not the IMPLY operation per sé.

For this work, this voltage was set to $V_{\text{reset}} = -1 \text{ V}$. Next, V_{set} and V_{cond} are determined. We define $V_{\text{set}} = 1 \text{ V}$, $V_{\text{cond}} = 0.9 \text{ V}$, based on the memristor's properties and Equations (1) and (2). With the voltages set, the constraints on R_G [30] can be evaluated, which leads to: $5.000 \text{ k}\Omega < R_G < 230.769 \text{ k}\Omega$. $R_G = 40 \text{ k}\Omega$ was chosen as the value of this resistor, which is lower than the geometric mean (100 k Ω) proposed by [43]. A summary of model and circuit parameters is shown in Table III, where the former are based on experimental results from previous works [18], [44].

Equations (4) and (9) are evaluated in order to get the operation constraints imposed by the circuit. Namely, $R_{\min,Q} = 101.449 \text{ k}\Omega$ and $s_{\min,Q} = 0.908$. We can see that, in Case 1 and assuming no state drift in P , the output memristor Q can never reach a state higher than $s_{\min,Q}$ or, equivalently, can never have a resistance lower than $R_{\min,Q}$.

B. Methodology & Setup

Proper IMPLY operation results – with respect to the output logic thresholds – are used to determine reliability. Correct operation is ensured when state changes within the memristors are occurring (switching conditions met) and are fast enough to exceed the given logic thresholds. We apply three different logic threshold schemes (shown in Figure 3) to evaluate the operation results in relation to the chosen logic threshold. Each scheme defines separate, normalized input ($s_{\text{IH}}, s_{\text{IL}}$) and output ($s_{\text{OH}}, s_{\text{OL}}$) thresholds, as in conventional

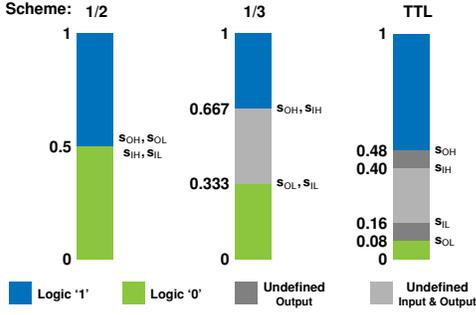


Figure 3. Different logic thresholds used in this paper.

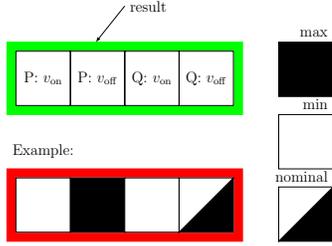


Figure 4. Four squares show the state of each variable in a simulation set and the outline color (green or red) shows the simulation result (correct or failed, respectively).

digital logic. Whereas the “1/2” and “1/3” scheme were chosen arbitrarily, the “TTL” scheme is derived from standard TTL ($V_{CC} = 5\text{ V}$) [45]. This is done by normalizing the threshold voltages V_{IH} , V_{IL} , V_{OH} and V_{OL} to V_{CC} – e.g. $s_{IH} = V_{IH}/V_{CC}$. The range between high and low thresholds, $[s_{IL}, s_{IH}]$ and $[s_{OL}, s_{OH}]$, is forbidden; in other words, the logic values and states in those ranges are considered undefined. Reasons for failures are not separately determined in our setup. Hence, failures during initialization, which lead to erroneous operation results, are counted as regular failures and are not distinguished from errors during the operation itself. Further, our simulation setup utilizes constant timesteps, so actual switching time are not explicitly measured.

To obtain a nominal timebase for the IMPLY gate, a transient analog simulation of the memristor model was conducted. Examining the resulting waveform of the normalized state s after the simulation showed that it takes $15\ \mu\text{s}$ to switch from 1% to 99% of the state boundaries. Thus, the timestep of circuit operation is set to $T = 15\ \mu\text{s}$. Every action (initialization, IMPLY operation, readout) is executed using this fixed timestep.

Analog transient simulations were conducted in LTSpice, making use of this setup. Two memristor parameters per device (R_{on} , R_{off} or v_{on} , v_{off} or k_{on} , k_{off}) were varied simultaneously within the ranges reported in measurements [21] and relative to the nominal state with a maximum deviation of $\pm 50\%$.

C. Result Presentation Method

To display the numerous results, we have come up with a presentation method of our own, which we introduce here.

Each parameter set is represented by a group of four squares. The left two squares, as displayed in Figure 4, show

parameter values of memristor P , and the right two show that of memristor Q . The filling of each square represents the state of the corresponding parameter: empty means minimum, half-filled nominal and fully filled maximum. Figure 4 shows this concept and provides an example, too. The outline color of the squares shows whether the simulation result for a set of parameter variation (Δ) was correct (highlighted by green) or incorrect (highlighted by red). In general, any combination of four parameters can be varied concurrently and displayed this way. However, our approach was to use three parameter sets: $\{R_{on,P}, R_{off,P}, R_{on,Q}, R_{off,Q}\}$, $\{v_{on,P}, v_{off,P}, v_{on,Q}, v_{off,Q}\}$ and $\{k_{on,P}, k_{off,P}, k_{on,Q}, k_{off,Q}\}$, as explained in Section V-B. Figure 5 shows a complete set of simulations for the parameters $\{v_{on,P}, v_{off,P}, v_{on,Q}, v_{off,Q}\}$. These resulting sets are then used to quickly identify those parameters that are common between different failed runs. For example, Figure 5 shows that the IMPLY operation produces no correct output if either, $v_{on,Q}$ or $v_{on,P}$, is at its maximum value for variations greater than or equal to 10%.

D. Results analysis

Combining the math provided in Section IV and the simulation results obtained in Section V-C into joint graphs gives us Figures 6 to 10. First, we take a closer look at Figures 6, 9 and 10, because they represent the most relatable logic threshold scheme, derived from traditional TTL thresholds. Figures 7 and 8 show the same equations as in Figure 6, plotted for the 1/2 and 1/3 threshold scheme, respectively. The other two graphs for these logic threshold schemes are omitted as they lead to the same conclusions as Figures 7 and 8. Furthermore, the threshold voltages turned out to be the most critical parameters, so special attention is given to their results.

1) *Graph structure:* Here, we explain how these graphs are composed. Parameters $R_{on,P}$ and $R_{off,P}$ of memristor P are always shown on the y-axis since R_P is crucial for the outcome of the operation. We can also see that from the fact that $R_{off,P}$ or $R_{on,P}$ are present in all of the constraints described in Section IV. Different parameters are used in each graph for the x-axes.

Colored curves and areas are used to show constraints and important ranges:

- Black, dashed lines indicate nominal parameter values
- Light blue lines show input logic thresholds R_{IH} (solid) and R_{IL} (dashed) for memristor P .
- Colored curves show the constraints from Section IV. Dotted parts indicate invalid plotting ranges, which do not correspond to any real value in physical devices.
- Arrows indicate how the constraints restrict the operating area of a parameter, i.e., which side of the curve is acceptable due to the given constraint.
- Blue areas show valid ranges of $R_{off,P}$ and the respective parameters on the x-axes. For example, in Figure 6, this area represents valid ranges of $R_{off,P}$ versus $v_{on,Q}$, $v_{off,Q}$, $v_{on,P}$ and $v_{off,P}$. Note that for $v_{on,P}$ our recommended range was used to limit the valid area, as the three different curves are only weak constraints.

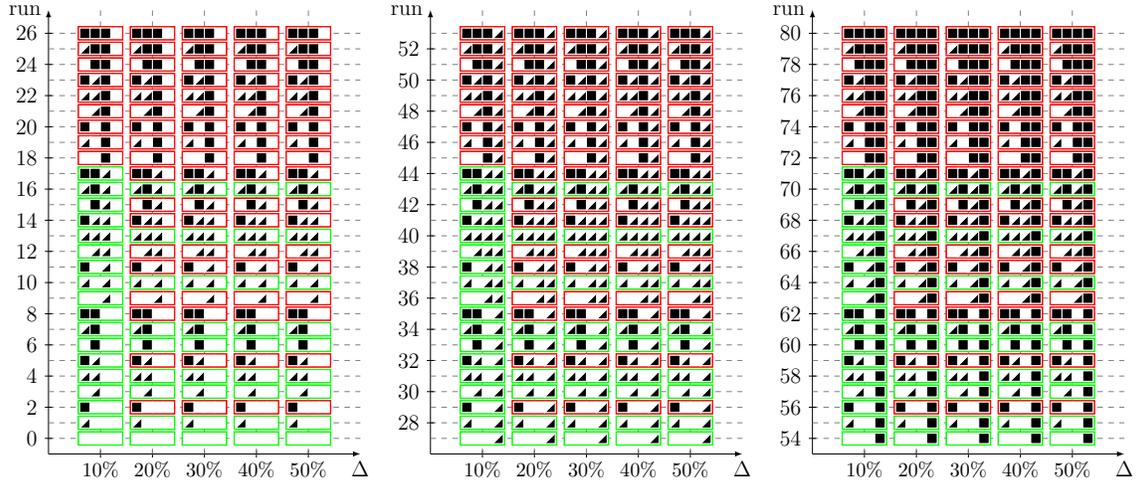


Figure 5. Results summary for different degrees of variation in v_{on} , v_{off} of P and Q . The 1/3 logic thresholds scheme was used here.

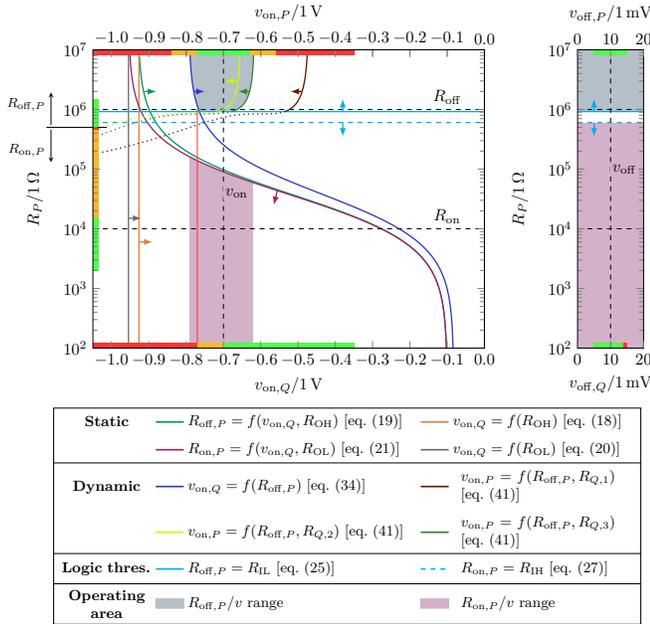


Figure 6. Analytical constraints and logic thresholds for the TTL scheme plotted over a range of memristor parameters $\{R_P, v_P, v_Q\}$.

- Purple areas show valid ranges of $R_{on,P}$ and the respective parameters on the x-axes. For example, in Figure 10, this area represents valid ranges of $R_{on,P}$ versus $k_{on,Q}$, $k_{off,Q}$, $k_{on,P}$ and $k_{off,P}$. Note that restrictions on x-axis parameters are inherited from the $R_{off,P}$ operating area.
- ■ The bars at each side of the graphs overlay our simulation results. Red sections show incorrect IMPLY results, green sections show correct results and orange sections are used for ranges in between, which are not explicitly covered by the simulations.

2) *Variation in voltage threshold:* Figures 6 to 8 depict voltage thresholds $v_{on,P}$, $v_{off,P}$, $v_{on,Q}$ and $v_{off,Q}$ of memristor P and Q , as well as resistance parameters $R_{on,P}$ and $R_{off,P}$ of P using different logic threshold schemes (Figure 3). For

the analysis we concentrate on the TTL scheme, Figure 6.

The logic thresholds (R_{IH} , R_{IL}) divide the plot into two parts: The bottom part concerning $R_{on,P}$ and the top part concerning $R_{off,P}$. Adding the static constraints, Equations (18) to (21), on top of the logic thresholds decreases the valid range of $R_{off,P}$, $v_{on,Q}$ and in particular $R_{on,P}$. The latter is evident from the purple area in Figure 6, which is smaller than the plotted range. However, regarding $R_{off,P}$ and $v_{on,Q}$, the dynamic constraint, Equation (34), is even stricter than the static constraint.

There are no static constraints for $v_{on,P}$. A rough dynamic estimation is provided by Equation (41), which depends on V_{Pf} . As discussed in Section IV-B, Equation (41) is evaluated three times, using $R_{Q,1}$, $R_{Q,2}$ and $R_{Q,3}$, respectively. The three curves are drawn in brown, dark green and light green. No constraint for v_{off} has been found (Section IV). Hence, the valid ranges of R_P over $\{v_{off,P}, v_{off,Q}\}$ are only limited by logic thresholds, Equations (25) and (27). As a consequence of the above constraints, the valid range for each parameter is decreased and thus the advisable operating area remains as shown by the colored areas.

Simulation results for variation in $v_{on,Q}$ show very good agreement with the mathematical analysis, especially the dynamic estimation in Equation (34), which depends on Equations (29) and (32). At +10% variation of $v_{on,Q}$ and nominal $R_{off,P}$, the simulation fails (indicated by the thin red line), as the analysis predicted. Figure 6 shows very clearly that this failure is not accurately predicted by the static constraints from Section IV-A alone. Hence, the dynamic estimation (Section IV-B) is vital. Variation in $v_{on,P}$ strengthens this point further, since different methods of estimating the dynamic behavior leads to important changes regarding the agreement of the simulations and the derived analytical constraints. On the upper end of the $v_{on,P}$ range, Equation (41) (evaluated using $R_Q = R_{Q,3}$ for V_{Pf} , Equation (35)) provides good congruence with our simulations, whereas Equation (41) (evaluated using $R_Q = R_{Q,2}$ for V_{Pf} , Equation (35)) represents a more conservative estimation. In contrast, evaluating Equation (41)

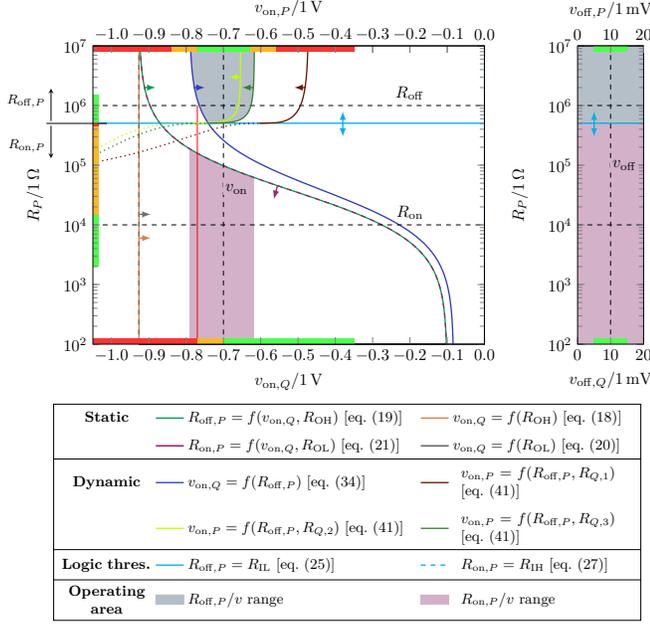


Figure 7. Analytical constraints and logic thresholds for the 1/2 scheme plotted over a range of memristor parameters $\{R_P, v_P, v_Q\}$.

using the theoretical minimum $R_Q = R_{Q,1} = R_{\min,Q}$ in Equation (35), does not yield a good estimation. On the lower end of the $v_{on,P}$ range, simulation results indicate some failures for $v_{on,P} \leq -0.84$ V (+20%). This behavior cannot be explained by any of the constraints from Section IV. According to the simulation results (Section V-C, Figure 5), these specific failures only occur when $v_{on,Q} \geq -0.7$ V ($\pm 0\%$), which leads us to believe that the reason for failure is the 20% mismatch between $v_{on,P}$ and $v_{on,Q}$. Regarding both, $v_{off,P}$ and $v_{off,Q}$, there are almost no failures as expected, except for a (minor) failure during initialization for $v_{off,Q}$ at +50%.

In terms of R_P variation, the simulation results suggest that $R_{off,P}$ can lie within the uncertain range between logic thresholds while the IMPLY operation still outputs correct results. This stands to reason since the thresholds are artificial limits not governed by the circuit behavior. Further, $R_{on,P}$ is fine up to the lowest simulated value of $R_{off,P}$, because at that point $R_{off,P} > R_{on,P}$ changes to $R_{off,P} < R_{on,P}$, and hence the operation fails.

Combining all the simulation results and their respective analytical constraints, we can identify the areas in which the circuit is most likely to operate correctly. These are the areas highlighted in Figures 6 to 8. Equations (34) and (41) and their respective dependencies, Equations (29), (32) and (35) (evaluated using $R_Q = R_{Q,3}$), are recommended for estimating the valid ranges of $R_{off,P}$ versus $\{v_{on,P}, v_{on,Q}\}$; whereas the static constraints Equations (18) to (21) are sufficient for $R_{on,P}$ versus $\{v_{on,P}, v_{on,Q}\}$.

3) *Variation in resistance limits:* There are no static constraints limiting $R_{on,Q}$ or $R_{off,Q}$. Therefore, only logic thresholds and the dynamic estimation of Equation (34) can be applied. The latter depends on Equations (29) and (32) and is evaluated in two ways: First, varying $R_{on,Q}$, but not $R_{off,Q}$; and second varying $R_{off,Q}$, but not $R_{on,Q}$. It is interesting to

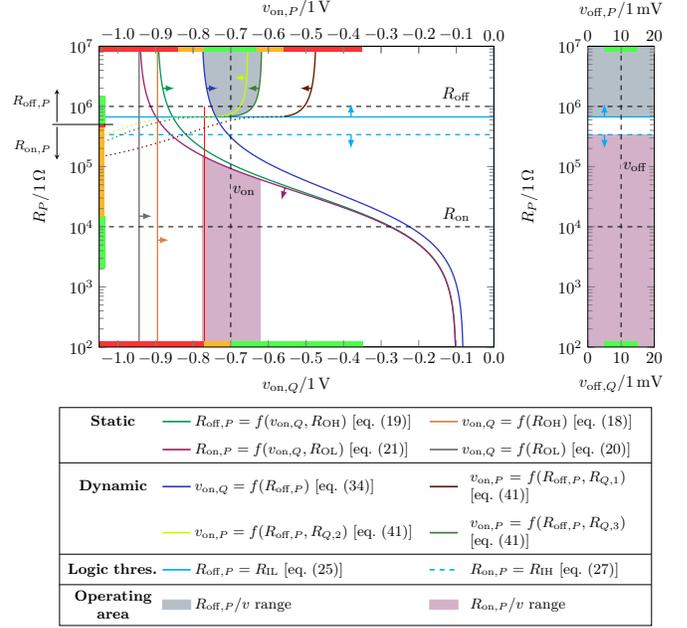


Figure 8. Analytical constraints and logic thresholds for the 1/3 scheme plotted over a range of memristor parameters $\{R_P, v_P, v_Q\}$.

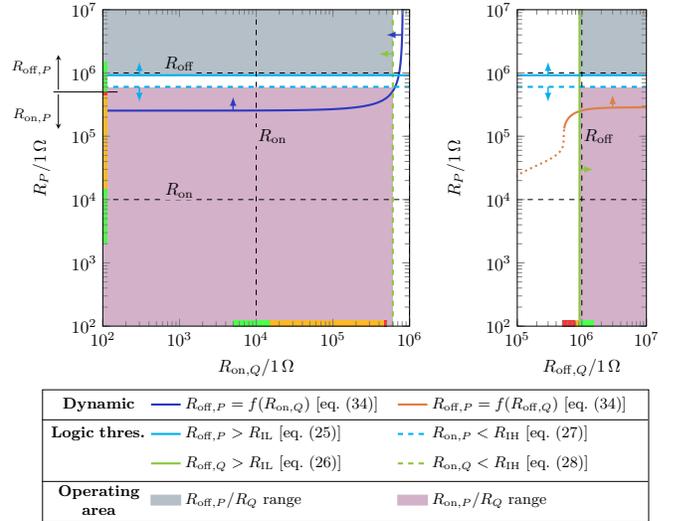


Figure 9. Analytical constraints and logic thresholds for the TTL scheme plotted over a range of memristor parameters $\{R_P, R_Q\}$.

see that – for any of the three schemes of Figure 3 – the logic thresholds limit the operating areas (blue and purple) much more than the actual analytical constraints. Simulation results for $R_{on,P}$ and $R_{off,P}$ are identical to Figure 6, however, $R_{off,Q}$ cannot reach as low as $R_{off,P}$ without causing a failure. This is solely due to the chosen logic thresholds, as an IMPLY output of $R_{off,Q} < R_{OL}$ is considered as failure.

Overall, resistance variation does not seem to hold as much potential for failures as variation in threshold voltage(s) does. Equation (34) and its dependencies, Equations (29) and (32), can be used to identify valid parameter ranges, but – based on our simulation results – it is most likely not necessary. This is true for all three logic threshold schemes listed in Figure 3.

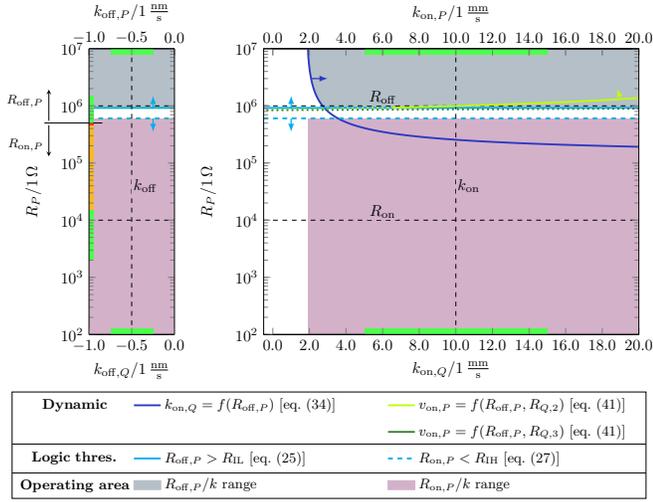


Figure 10. Analytical constraints and logic thresholds for the TTL scheme plotted over a range of memristor parameters $\{R_P, k_P, k_Q\}$.

4) *Variation in switching speed*: The dynamic constraint in Equation (34) can be used to extract limits of $k_{on,Q}$, while Equation (41) provides the basis for the analysis of $k_{on,P}$. Figure 10 shows the plotted equations and logic thresholds. Equation (41) (evaluated using Equation (35), where $R_Q = R_{Q,1}$) is omitted, as well as all constraints containing $k_{off,P}$ and $k_{off,Q}$, since they are far outside of the plotted range. The graph in Figure 10 shows that $k_{on,P}$ is hardly restricted by any constraint. Only at relatively high values, greater than +50% variation, Equation (41) (evaluated using Equation (35) with $R_Q = R_{Q,2}$) comes into effect, but cannot be compared to simulation results, as our simulated range ends at +50%, in compliance with our methodology (Section V-B). In contrast, Equation (34) provides a reasonable constraint for $k_{on,Q}$. Nonetheless, our simulated range only reaches down to -50% and thus results cannot be compared to the constraint. The other two logic threshold schemes show similar behavior. As before, the colored areas indicate the merged, predicted functional range of both, $k_{on,P}$ and $k_{on,Q}$.

In conclusion, switching speed k of both memristors can vary at least by $\pm 50\%$ without performance issues, according to our simulation. Analytical constraints suggest that there is a lower boundary for $k_{on,Q}$ at approximately 2 mm/s (-80%).

VI. SIMULATION – CROSSBAR

A. Setup

Analogous to the single IMPLY gate simulation setup (Section V-A), the circuit in Figure 1(b) is the basis for the crossbar simulation. A complete 128×128 cell 1T1R crossbar circuit was used. The IMPLY gate is formed by two memristors arbitrarily located within the crossbar. Each memristor has its own access device, in our case an ideal switch, and is connected to adjacent cells via resistors that model the nanowire resistances. The ideal switch is modeled using an on-resistance of $1 \mu\Omega$ and an off-resistance of $100 \text{ M}\Omega$. Line resistances were chosen to be 10Ω each, according to the worst case in [26]. Figure 11 shows the structure of a single cell.

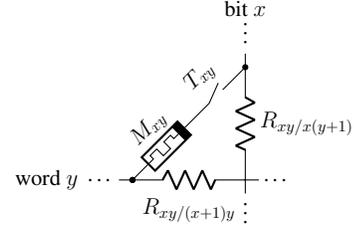


Figure 11. Structure of a single cell within the 1T1R crossbar, including line resistances.

Circuit parameters of the IMPLY gate are identical to Section V-A, Table III. Bit-line drivers are attached at the top and bottom for symmetry. The readout strategy described in Section II-B was implemented. Analog transient simulations were conducted in Cadence Spectre. The method of parameter variation is the same as defined for the single gate in Section V-B, except that only relative parameter variations ($\pm 50\%$) were conducted for the crossbar.

B. Methodology

IMPLY gates can be formed by any two memristors in the crossbar. Both, the worst case scenario in terms of parasitic resistance between the two memristors forming a gate, and the worst case voltage drop, were considered. Hence, four separate simulations were conducted with P and Q at different {bit, word} positions.

- 1) Memristor P at position $\{0, 0\}$, Q at position $\{127, 127\}$
- 2) Memristor P at position $\{127, 127\}$, Q at position $\{0, 0\}$
- 3) Memristor P at position $\{0, 0\}$, Q at position $\{63, 63\}$
- 4) Memristor P at position $\{63, 63\}$, Q at position $\{0, 0\}$

Instead of using idealized ($s = 0$ or $s = 1$) or manually fixed initial memristor states, each cell is assigned a different initial state during (automated) netlist generation. The states are generated via Octave and follow a Gaussian distribution which has been cut in half as shown in Figure 12. Although this approach requires a greater effort, it represents a more realistic scenario than ideal initial states.

C. Results analysis

In this section we compare the crossbar simulation results against the single gate results. As before, to be efficient, results are represented using our technique introduced in Section V-C. Figure 13 shows a complete set of crossbar simulations for the parameters $\{v_{on,P}, v_{off,P}, v_{on,Q}, v_{off,Q}\}$. Figure 14 depicts the combined, i.e. worst case, results of all crossbar simulation

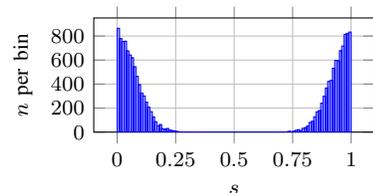


Figure 12. Histogram of initial (normalized) device states, s , within the 128×128 crossbar, plotted using 100 bins.

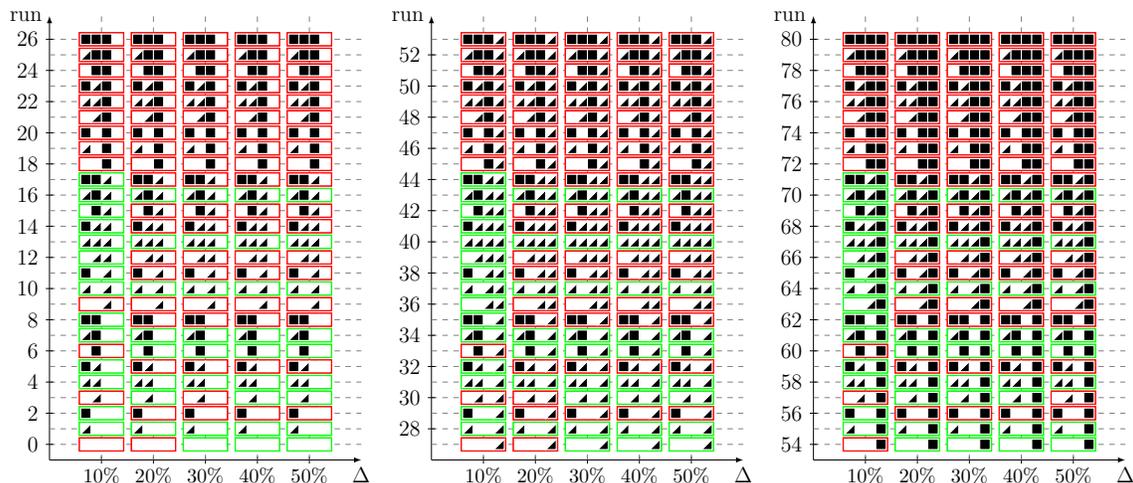


Figure 13. Crossbar results summary for different degrees of variation in v_{on}, v_{off} of P and Q . Logic thresholds for ‘1’ and ‘0’ were set according to the TTL threshold scheme (Figure 3). Memristor P was at position $\{0,0\}$, while Q was at the center, $\{63,63\}$.

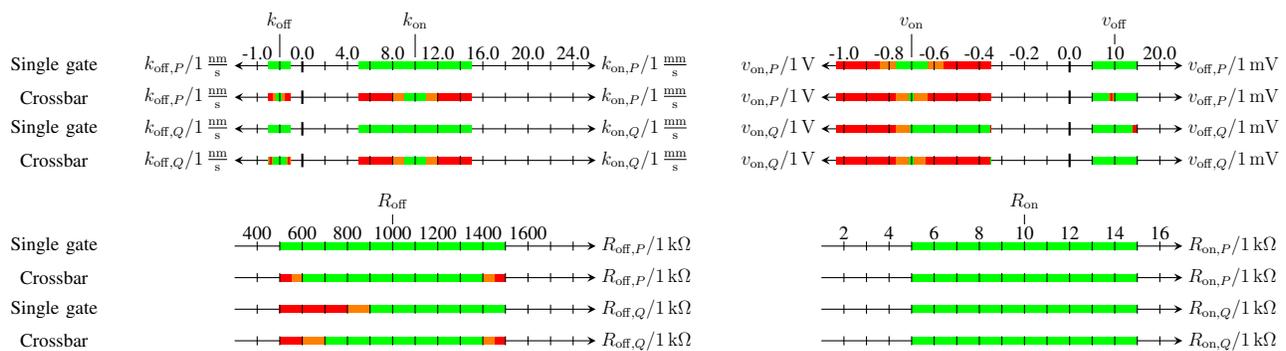


Figure 14. Comparison of single gate and (combined) crossbar simulation results. A range of $\pm 50\%$ around the nominal value is plotted for each parameter. The results are color-coded: Green for correct IMPLY output, red for false output and orange for ranges in-between, that are not covered by the simulation.

setups explained in Section VI-B, and the results of the single gate simulation, where the TTL threshold scheme was applied. The bars and color coding are identical to Figures 6 to 10, Section V-D. While the conclusions from Section V-D remain true, unless noted otherwise, here we highlight the differences.

1) *Variation in voltage threshold:* Given that the circuit is in a crossbar architecture, an increased number of errors due to threshold voltage variation can be expected in the crossbar simulation, when compared to the single gate simulation. Surprisingly, however, it is not significantly worse.

There are three main differences: First, the initialization failure of $v_{off,Q}$ (initially shown in Figure 6) does not arise in the crossbar simulation. However, there were initialization failures in the crossbar for $8 \text{ mV} \leq v_{off,P} \leq 9 \text{ mV}$ (-20% to -10%). Having said that, as v_{off} is of minor interest to the IMPLY operation, this can neither be considered an improvement, nor a degradation compared to the single gate. Second, results indicate failures if both $v_{on,P}$ and $v_{on,Q}$ are above -0.63 V (-10%) at the same time. Based on the single gate simulation results (Section V-D) and our recommendation to use Equation (41) – in combination with $R_Q = R_{Q,3}$ in Equation (35) – for device variability evaluation, this failure is predictable. As for the exact reason of this error, we assume

that it is due to the increased state drift in P , as $|v_{on,P}|$ is so low. In terms of operational range, the valid values for $v_{on,P}$ and $v_{on,Q}$ are drastically restricted to the nominal value v_{on} , as shown in Figure 14. It is only then that correct operations can be guaranteed. However, if $v_{on,P} < -0.63 \text{ V}$ (-10%) is ensured, a much greater range for $v_{on,Q}$ is admissible, similar to the case of the single gate in Section V-D. Finally, the third difference is that the IMPLY operation fails for $v_{on,P} < -0.77 \text{ V}$ ($+10\%$) while $v_{on,Q} = v_{on}$, as compared to $+20\%$ in the single gate simulation. Thus, the tolerable mismatch between $v_{on,P}$ and $v_{on,Q}$ shrinks to 10% within the crossbar.

Apart from these differences the results of both simulations are identical, although Figure 14 might not reveal it at the first look. This means that the proposed constraints for v_{on} and v_{off} from Section IV can be applied to get a basic understanding of threshold voltage variability within crossbar architectures.

2) *Variation in resistance limits:* Varying the resistance limits of the memristors within the crossbar reveals some interesting results, as we can see in Figure 14. While IMPLY operations in the single gate simulation fail for $R_{off,Q} \leq 800 \text{ k}\Omega$ (-20%), the crossbar simulation shows correct results down to $R_{off,Q} = 700 \text{ k}\Omega$ (-30%). We believe that this is

due to the readout strategy applied to the crossbar, since the measured R_Q after executing Case 3 (Table I) is almost $1\text{ M}\Omega$ in a majority of the -30% simulation runs. Failures start occurring below $R_{\text{off},Q} \leq 600\text{ k}\Omega$ (-40%). The range between -30% and -40% variation is not explicitly covered by our simulation steps.

Furthermore, false IMPLY results within the crossbar come about at the upper and lower end of our simulated $R_{\text{off},Q}$ range, as well as at the upper and lower end of the simulated $R_{\text{off},P}$ range. This is a combined effect, since those errors only occur if both, $R_{\text{off},P} \leq 500\text{ k}\Omega$ (-50%) and $R_{\text{off},Q} \geq 1.5\text{ M}\Omega$ ($+50\%$), or vice versa, are present at the same time. Interpreting this scenario based on the 1/2 or TTL logic thresholds from Figure 3, one can see that if either $R_{\text{off},P}$ or $R_{\text{off},Q}$ are below $500\text{ k}\Omega$, they are not interpreted as logic ‘0’, but logic ‘1’. Thus, they do not fulfill Case 1 of the truth table, where $p = 0$ and $q = 0$ must be true. Applying the 1/3 logic threshold scheme, an off-resistance of $500\text{ k}\Omega$ yields an undefined logic state. Therefore, none of the cases in the truth table is fulfilled. Hence, such errors are predicted via logic thresholds alone and do not require further evaluation using the constraints defined in Section IV.

Lastly, we should remark that simulation results for $R_{\text{on},P}$ and $R_{\text{on},Q}$ in the crossbar are identical to the the single gate simulation results.

3) *Variation in switching speed*: Switching speed variation does not pose a threat to single IMPLY gates, as deduced in Section V-D. However, based on our simulation results (Figure 14), behavior within a crossbar is very different. For variations in $k_{\text{on},P}$ and $k_{\text{on},Q}$ larger than $\pm 20\%$, the IMPLY operation fails. Further analysis of those failures reveals that it is the mismatch between P and Q which causes most errors. If either $\Delta k_{\text{on},P} \leq -20\%$ while $\Delta k_{\text{on},Q} \geq +20\%$, or $\Delta k_{\text{on},P} \geq +20\%$ while $\Delta k_{\text{on},Q} \leq -20\%$, the operation result is wrong. This mismatch cannot be predicted by our constraints. Further, the simulation indicates failures for variation in $k_{\text{off},P}$ larger than $\pm 20\%$, as well as for $\Delta k_{\text{off},Q} = \pm 40\%$. As $k_{\text{off},P}$ and $k_{\text{off},Q}$ are never relevant during IMPLY, we infer that these are initialization errors. They can, however, be resolved by using a different initialization scheme than the one we applied. For example, using an additional readout cycle to confirm written initial states. Such a scheme provides feedback to resolve initialization errors before IMPLY is executed.

VII. CONCLUSION

Device variability is one of the main challenges when implementing memristor-based logic. In this paper, we formulated novel constraints based on static switching conditions and state change dynamics. We note that the underlying causes of variation in device parameters are not differentiated by our methodology. Hence, environmental effects (such as temperature) causing parameter variation are taken into account by our constraints, just as process variations are. IMPLY operation results after a fixed timestep of execution were used as the metric to assess gate performance. In addition, different logic threshold schemes were considered. The derived constraints were put to the test in an extensive analysis for single gate

and 128×128 1T1R crossbar and their simulation results were compared. An efficient simulation results presentation method was introduced and applied to find critical parameters.

As a result of our analysis, variability in threshold voltages, especially $v_{\text{on},Q}$, was identified as a major root of concern regarding correct operations. We conclude that the most dominant reasons for failure are predictable by our theoretical analysis for both the single gate and the crossbar. Therefore, our analysis and recommendations can be used for designing a reliable IMPLY gate. More specifically, we suggest to choose design parameters away from the borders of the recommended areas. Ideally, this distance should be chosen such that the typical (or maximum) variations, do not lead to crossing the borders of recommended area. Nonetheless, accompanying studies or simulations should be conducted to understand the non-deterministic errors, especially regarding voltage threshold- and switching speed mismatch within the crossbar, as well as state drift phenomena.

Lastly, we note that our analysis can be used to decide whether a specific memristor technology and IMPLY logic are compatible. To that end, technology parameters need to be assessed based on the constraints for reliable IMPLY operations we extracted in this work. Further, considering technology-dependent parameter variation, an acceptable margin from the borders of the operating area must be ensured. Otherwise, chances for failures in IMPLY operations are increased. Hence, it would be better to use other technologies to implement the intended IMPLY-based circuits, or use other logics to implement the intended functionalities on the given technology.

REFERENCES

- [1] D. Niu *et al.* Low-power dual-element memristor based memory design. In *Proceedings of the 16th ACM/IEEE International Symposium on Low Power Electronics and Design, ISLPED '10*, pp. 25–30, New York, NY, USA, 2010. ACM.
- [2] Y. Ho *et al.* Dynamical properties and design analysis for nonvolatile memristor memories. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(4):724–736, April 2011.
- [3] B. Mohammad *et al.* Robust hybrid memristor-CMOS memory: Modeling and design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 21(11):2069–2079, November 2013.
- [4] V. S. Baghel and S. Akashe. Low power memristor based 7T SRAM using MTCMOS technique. In *Fifth International Conference on Advanced Computing Communication Technologies*, pp. 222–226, February 2015.
- [5] D. Radakovits and N. TaheriNejad. Implementation and characterization of a memristive memory system. In *2019 IEEE 32nd Canadian Conference on Electrical and Computer Engineering (CCECE)*, pp. 1–5, May 2019.
- [6] M. Zangeneh and A. Joshi. Design and Optimization of Nonvolatile Multibit 1T1R Resistive RAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(8):1815–1828, Aug 2014.
- [7] H. Kim *et al.* Memristor-based multilevel memory. In *CNNA2010*, pp. 1–6, Feb 2010.
- [8] N. Taherinejad *et al.* Memristors’ potential for multi-bit storage and pattern learning. In *EMS2015*, pp. 450–455, Oct 2015.
- [9] N. Taherinejad *et al.* Fully digital write-in scheme for multi-bit memristive storage. In *CCE2016*, pp. 1–6. IEEE, 2016.
- [10] Y. Pershin and M. Di Ventra. Neuromorphic, digital, and quantum computation with memory circuit elements. *Proceedings of the IEEE*, 100(6):2071–2080, June 2012.
- [11] A. Thomas. Memristor-based neural networks. *Journal of Physics D: Applied Physics*, 46(9):093001, 2013.
- [12] J. Borghetti *et al.* ‘Memristive’ switches enable ‘stateful’ logic operations via material implication. *Nature*, 464:873–876, April 2010.

- [13] N. Talati *et al.* Logic Design Within Memristive Memories Using Memristor-Aided loGIC (MAGIC). *IEEE Transactions on Nanotechnology*, 15(4):635–650, July 2016.
- [14] E. Linn *et al.* Complementary resistive switches for passive nanocrossbar memories. *Nature Materials*, 9:403–406, May 2010.
- [15] S. Gupta *et al.* FELIX: Fast and energy-efficient logic in memory. In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 1–7, November 2018.
- [16] G. Papandroulidakis *et al.* Crossbar-based memristive logic-in-memory architecture. *IEEE Transactions on Nanotechnology*, 16(3):491–501, May 2017.
- [17] S. G. Rohani and N. TaheriNejad. An improved algorithm for IMPLY logic based memristive full-adder. In *2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE)*, pp. 1–4, April 2017.
- [18] N. TaheriNejad *et al.* A semi-serial topology for compact and fast IMPLY-based memristive full adders. In *2019 IEEE New Circuits and Systems symposium (NewCAS)*, pp. 1–5, 2019.
- [19] L. Guckert and E. E. Swartzlander Jr. *System design with memristor technologies*. Institution of Engineering & Technology, 2018.
- [20] D. Radakovits *et al.* A memristive multiplier using semi-serial imply-based adder. *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–12, 2020.
- [21] N. TaheriNejad and D. Radakovits. From behavioral design of memristive circuits and systems to physical implementations. *IEEE Circuits and Systems Magazine*, 19(4):6–18, Fourthquarter 2019.
- [22] R. Waser *et al.* Redox-based resistive switching memories – nanoionic mechanisms, prospects, and challenges. *Advanced Materials*, 21:2632–2663, 2009.
- [23] S. Menzel *et al.* Switching kinetics of electrochemical metallization memory cells. *Physical Chemistry Chemical Physics*, 2013. Cite this: *Phys. Chem. Chem. Phys.*, 2013, 15, 6945.
- [24] S. Menzel *et al.* Physics of the Switching Kinetics in Resistive Memories. *Advanced Functional Materials*, 25:6306–6325, 2015.
- [25] Y. Cassuto *et al.* Sneak-Path Constraints in Memristor Crossbar Arrays. *IEEE International*, pp. 156–160, 2013.
- [26] M. A. Zidan *et al.* Memristor multiport readout: A closed-form solution for sneak paths. *IEEE Transactions on Nanotechnology*, 13(2):274–282, March 2014.
- [27] N. Wald and S. Kvatinsky. Understanding the influence of device, circuit and environmental variations on real processing in memristive memory using Memristor Aided Logic. *Microelectronics Journal*, 86:22–33, February 2019.
- [28] L. Xie *et al.* On the robustness of memristor based logic gates. In *2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, pp. 158–163, April 2017.
- [29] Q. Chen *et al.* A Logic Circuit Design for Perfecting Memristor-Based Material Implication. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 36(2):279–284, February 2017.
- [30] S. Kvatinsky *et al.* Memristor-based imply logic design procedure. *IEEE 29th International Conference on Computer Design (ICCD)*, pp. 142–147, 2011.
- [31] H. Wan *et al.* In situ observation of compliance-current overshoot and its effect on resistive switching. *EDL2010*, 31(3):246–248, 2010.
- [32] C. Li *et al.* In-memory computing with memristor arrays. In *IMW2018*, pp. 1–4. IEEE, 2018.
- [33] C. Li *et al.* Analogue signal and image processing with large memristor crossbars. *Nature Electronics*, 1(1):52, 2018.
- [34] A. Chen. A comprehensive crossbar array model with solutions for line resistance and nonlinear device characteristics. *IEEE Transactions on Electron Devices*, 60(4):1318–1326, April 2013.
- [35] S. Shin *et al.* Analysis of passive memristive devices array: Data-dependent statistical model and self-adaptable sense resistance for rams. *Proceedings of the IEEE*, 100(6):2021–2032, 2012.
- [36] S. Shin *et al.* Data-dependent statistical memory model for passive array of memristive devices. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(12):986–990, December 2010.
- [37] S. Kvatinsky *et al.* TEAM: Threshold Adaptive Memristor Model. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 60(1):211–221, January 2013.
- [38] S. Kvatinsky *et al.* VTEAM: A General Model for Voltage-Controlled Memristors. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 62(8):786–790, August 2015.
- [39] J. P. Strachan *et al.* State dynamics and modeling of tantalum oxide memristors. *IEEE Transactions on Electron Devices*, 60(7):2194–2202, July 2013.
- [40] Z. Jiang *et al.* A compact model for metal–oxide resistive random access memory with experiment verification. *IEEE Transactions on Electron Devices*, 63(5):1884–1892, May 2016.
- [41] D. Radakovits *et al.* Second (v2.0) LTSpice implementation of VTEAM, September 2019. <https://www.ict.tuwien.ac.at/staff/taherinejad/projects/memristor/files/vteam2.asc>, <https://www.ict.tuwien.ac.at/staff/taherinejad/projects/memristor/files/vteam2.asy>.
- [42] Knowm. *Known Self Directed Channel Memristors*, October 2019. Rev. 3.2, https://knowm.org/downloads/Known_Memristors.pdf, Last accessed: 11 March 2020.
- [43] S. Kvatinsky *et al.* Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(10):2054–2066, October 2014.
- [44] S. G. Rohani *et al.* A semiparallel full-adder in imply logic. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, pp. 1–5, 2019.
- [45] Texas Instruments. *Logic Guide*, 2017. <http://www.ti.com/lit/sg/sdyu001ab/sdyu001ab.pdf>, Last accessed: 11 March 2020.



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