Adaptive Impedance Matching for Vehicular Power Line Communication Systems

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***Abstract*—The growing number of electronic devices inside vehicles has motivated research and development activities in Vehicular Power Line Communication (VPLC) systems. Advantages of the VPLC approach include reduced complexity and cost of the wiring harness. Among the design challenges of VPLC systems is the problem of impedance matching. The access impedance at the modem port is a time varying quantity which also depends on the location of the VPLC modem. Impedance mismatch degrades the signal-to-noise ratio (SNR) and thus the signal integrity. Given the variable nature of the access impedance, a fixed matching circuit will be inefficient. A potential solution to cope with the access impedance variability is an adaptive impedance matching system which is the subject of this work. Here we have designed an adaptive impedance matching system. The system is simulated and its performance is evaluated under extreme changes in access impedance.**

I. Introduction

The concept of using supply wires for communication purposes is not a new concept and has been already applied for various applications including smart girds and in-house applications [1]. With the exponential growth in the number of electronic devices in vehicles [2], using power line communication (PLC) in vehicles has attracted the attention of many researchers and practitioners, cf. e.g., [3]–[7]. It has been estimated that two billion nodes of electronic devices will be connected through the vehicular electrical network by 2014 [8]. Thus, vehicular PLC (VPLC) is becoming a more appealing solution for decreasing the complexity and cost of the wiring network inside vehicles [2], [9]. However, the development of reliable VPLC solutions faces several challenges, including the presence of impulsive noise and the location and time-variant nature of the access impedance, as well as its frequency selectivity [1, Ch. 4], [10], [11]. Impedance mismatch degrades the PLC signal strength, and due to the changes of the access impedance, simple matching circuits with fixed passive elements are inefficient [10].

In this paper, as a continuation of our previous work [12], we present an adaptive impedance matching solution for VPLC systems. For the design we use in-vehicle access impedance values obtained from our measurement campaigns, whose results were presented in [11], [13]. The performance of our solution is evaluated under extreme scenarios, considering boundary values of the measured impedance range. Some important characteristics of the system such as its bandwidth and delay are also derived and discussed. While adaptation is done for a nominal frequency, usually the carrier frequency of the communication signal, and thus the matching scheme is narrowband, sample numerical results indicate that the resulting matching circuit can be wideband for VPLC applications operating in the about 30-50 MHz range.

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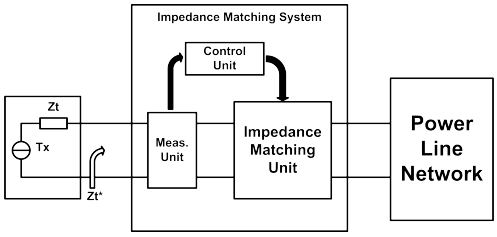

Fig. 1: Block diagram of an adaptive impedance matching system at the transmitter side.

The remainder of this paper is organized as follows. Section II discusses the design concept and methodology. Section III presents the test set-up as well as the simulation results of the proposed solution. Section IV concludes the paper.

II. An Adaptive Impedance Matching System for VPLC

The proposed adaptive impedance matching system consists of three main units: measurement unit, impedance matching unit and control unit. These building blocks are shown in Fig. 1.

A. Our Approach to the Matching Problem

The matching problem can be graphically explained using the Smith chart (see Fig. 2), as finding a circuit with which one can move from a given impedance, point A, to the desired impedance or destination, point B (typically the centre of the Smith chart). There are numerous solutions for this problem, however, to keep the solution lossless one needs to move along the contours of constant resistance and constant conductance. Although this limitation reduces the number of solutions, there are still a large number of possible paths. Two sample paths are depicted in Fig. 2. Each move on the contours represents a series or parallel non-resistive element in the matching circuit. Hence, the solution depicted in gray color (dotted line) consists

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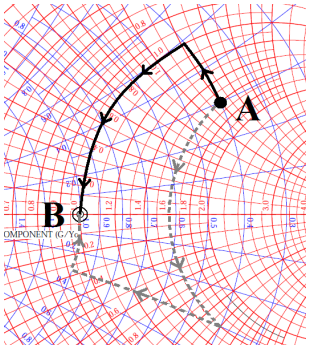

Fig. 2: Matching problem visualized in the Smith chart. Taking different paths from the given impedance point A to the desired impedance point B.

of three elements whereas the one in black (solid line) needs only two elements.

Therefore, limiting the number of moves on the Smith chart helps to keep the matching circuit simpler. This in turn reduces the complexity of the control unit since there will be fewer decisions to be made and fewer elements to control. Thus, a matching strategy similar to the solution depicted with the black contour (solid line) in Fig. 2 is chosen for the proposed system. That is, the first move according to the location of point A is on the constant conductance contour (via a parallel capacitor) or on the constant resistance contour (via a series inductor) to correct the real part of the impedance, and the second move is respectively on the constant resistance contour (using a series capacitor) or on the constant conductance contour (using a parallel inductor) to adjust the imaginary part.

B. The Components of the Matching System

Having established the basic principle applied to obtain impedance matching, we now explain the details of the three main components of the matching system shown in Fig. 1. To this end, we assume that our matching system is driven by a single-frequency signal at a frequency f_c. In a practical scenario, this could either be a dedicated preamble for the purpose of matching, or a communication signal at centre frequency f_c.

1) Measurement Unit: The measurement unit consists of a sensing unit and an interpretation unit as shown in Fig. 3.

The sensing unit circuitry is shown in Fig. 4. It consists of a resistor with a very small value (e.g., 1 Ω) and two operational amplifiers (op-amps) that are set up to measure the voltage across the resistor (which represents the current going through it) and the voltage difference between the input and the reference node (ground), which represents the voltage at the input of the matching system. Another task of the op-amps is amplifying the measured signals in order to make it possible for the interpretation unit to process them.

The interpretation unit receives the voltage and current signals generated by the measurement circuitry and outputs two control signals, V_{env} and P_{env}, that are used by the control unit (see Fig. 1). As shown in Fig. 5, a diode first rectifies the sinusoidal input which is then passed through an RC low-pass filter to extract the envelop of the input signal.

Referring to the Smith chart in Fig. 2, the first move is intended to be on the constant conductance contour, correcting the real part of the impedance. For this purpose, V_{env} is obtained applying the simple envelope detector circuit (Figure 5) to V_s (see Figure 4). The second output of the interpretation unit contains the information about the imaginary part of the access impedance or equivalently the phase information. For this purpose, the power variable P_{env} is generated at the output of the envelope detector circuit as shown in Fig. 5. In this case, the rectifier is fed with the multiplication of two inputs, i.e., current I_s and voltage V_s. Since the multiplication is performed before the rectification, this signal also represents the respective phase of voltage and current. To show this, let us assume the voltage and current which are measured by the sensing unit are the sinusoidal signals

$$I_s = \sqrt{2} I_0 \cos(2\pi f_c t) \quad (1)$$

$$V_s = \sqrt{2} V_0 \cos(2\pi f_c t + \phi) \; . \quad (2)$$

The product of these two signals, i.e., the power signal, can be expressed as

$$\begin{aligned} P_s &= 2KV_0 I_0 \cos(2\pi f_c t + \phi)\cos(2\pi f_c t) \\ &= KV_0 I_0 \cos(4\pi f_c t + \phi) + KV_0 I_0 \cos(\phi) \; , \end{aligned} \quad (3)$$

where K is a constant denoting the overall gain of the multiplier circuit. Therefore, at the output of the measurement unit we have

$$P_{env} = KV_0 I_0 (1 + \cos(\phi)) \; , \quad (4)$$

which includes the phase information.

Depending on the value of the V_{env}, one can infer whether the real part of the access impedance is larger or smaller than the desired matched impedance. To investigate this further, consider Fig. 6 where the network impedance is modelled as Z_{acc}. For simplicity, first let us assume Z_{acc} is purely resistive, i.e., $Z_{acc} = R_z$, in which case the voltage at the network load (whose magnitude is measured as V_{env} by the measurement unit) is

$$V_z = \frac{R_z}{R_g + R_z} V_g \; . \quad (5)$$

The optimum power transfer to the load Z_{acc} happens when $R_z = R_g$, for which

$$\frac{V_z}{V_g} = \frac{1}{2} \; . \quad (6)$$

If R_z is larger or smaller than R_g, then V_z is larger or smaller than the matched value.

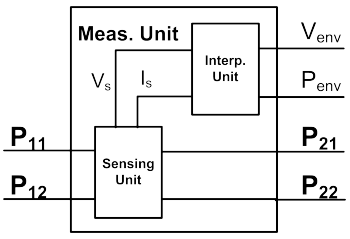

Fig. 3: Illustration of the measurement unit.

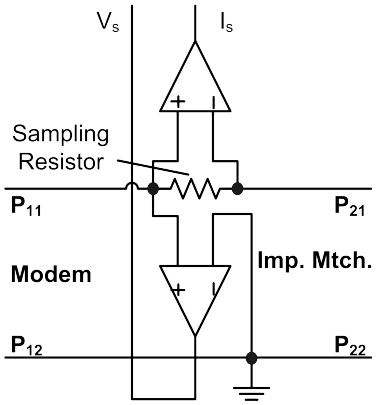

Fig. 4: Sensing unit circuitry including one resistor and two op-amps, connected to the modem at one end and to the Matching Unit on the other end.

Now for the general case, when Z_{acc} is a complex number, Eq. (5) can be re-written as

$$\frac{V_z}{V_g} = \frac{R_z + jX_z}{R_g + R_z + jX_z} \tag{7}$$

Considering the magnitude of (7), and solving it for smaller or equal to one half, we have

$$\left|\frac{V_z}{V_g}\right|^2 = \frac{R_z^2 + X_z^2}{(R_g + R_z)^2 + X_z^2} \leq \frac{1}{4} \tag{8}$$

$$\Leftrightarrow \quad 0 \leq R_g^2 + 2R_gR_z - 3R_z^2 - 3X_z^2 \tag{9}$$

$$\Rightarrow \quad R_z \leq R_g \ . \tag{10}$$

Hence, in both cases of purely resistive or complex access impedance, $|V_z| \leq \frac{1}{2}|V_g|$ can happen only if the real part of the network access impedance, R_z, is smaller than or equal to the transmitter output resistance, R_g. Therefore, if the measurement V_{env} is smaller than $1/2|V_g|$, it shows that resistance of the access impedance is too small and thus needs to be compensated by using a series inductor. While we do not have a similar relationship for when V_{env} is larger than $1/2|V_g|$, application of a parallel capacitor in our system has proven to be helpful in bringing V_{env} closer too $1/2|V_g|$.

Furthermore, referring to Eq. (4) and assuming that the voltage amplitude and the real part of the impedance have been optimized, a small amplitude for the power measurement P_{env} indicates a phase mismatch. This can be compensated for using a series capacitor or a parallel inductor corresponding to a larger or smaller than the ideal matched value of the voltage amplitude. Therefore the resulting structure of the impedance matching unit would be an L-shaped circuit.

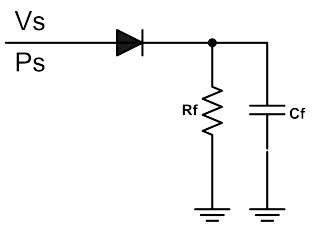

Fig. 5: Rectifying circuit and respective filter for the interpretation unit.

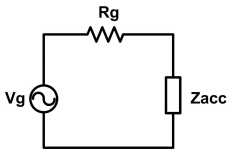

Fig. 6: Simplified matching problem where network impedance is modelled by Z_{acc}.

2) Matching Unit: As derived above, a subset of L-structured capacitors or inductors can match the impedance at source leading to the maximum power transfer from the source to the network. Therefore, a properly configured circuit as shown in Fig. 7 can match the source to the network.

3) Control Unit: Using the measured V_{env} and P_{env}, the control unit determines the position of the switches and the values of the components in the matching circuit shown in Fig. 7. If V_{env} is above a certain threshold, called V_{Up-Th}, the parallel capacitor "CP" in Fig. 7 should become active. Therefore, the respective switch, S_{MCp}, turns on. Simultaneously the P_{env} is compared with the respective threshold (P_{Th}) and if its value is below the threshold, S_{RCp} turns on and S_{RSw} turns off, otherwise S_{RSw} which is a normally closed switch remains on while S_{RCp} remains off. On the other hand, if V_{env} is below a lower threshold called V_{Lw-Th}, the series inductor "LS" should become active. Hence S_{LIn} turns on and consequently S_{LSw} turns off. Then P_{env} is compared to P_{Th}. S_{MIn} is turned on if $P_{env} < P_{Th}$ and otherwise it remains off. In all other cases not mentioned above all the switches keep their previous status, which are initially off, except for the S_{LSw} and S_{RSw} which are "normally on" switched and hence on at the beginning.

The threshold values V_{Up-Th}, V_{Lw-Th}, and P_{Th} are chosen based on the perfectly matched condition with allowance of 10% difference. These readings depend on the amplitude of the source voltage. Therefore they can be driven as following

$$V_{Th} = (1 \pm 0.1)\ A \cdot |\frac{Z_{acc}}{Z_g + Z_{acc}}| \cdot |V_g| \Big|_{Z_{acc}=Z_g^*} \tag{11}$$

$$\Rightarrow \quad V_{Up-Th} = 1.1\ \frac{A}{2}\ |V_g| \tag{12}$$

$$\Rightarrow \quad V_{Lw-Th} = 0.9\ \frac{A}{2}\ |V_g| \tag{13}$$

where A is the gain of measurement circuit. Similarly for P_{Th} we will have

$$P_{Th} = 1.1\ \frac{A}{2}\ |V_g \cdot I_g| \tag{14}$$

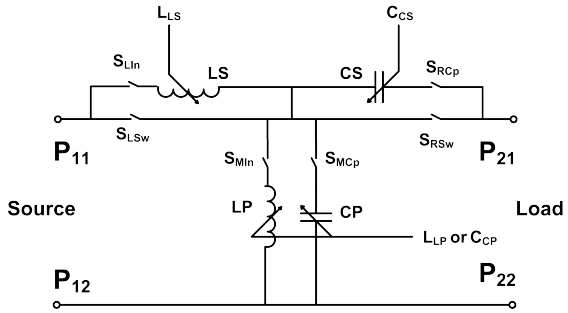

Fig. 7: Matching circuitry.

TABLE I: Logic table for switches where the bit stream represents the status of switches in following order from MSB to LSB "S_{LSw}, S_{LIn}, S_{MIn}, S_{MCp}, S_{RCp}, S_{RSw}"

On the rising edge of "Adj"	$P_{s-dc} > P_{Th}$	$P_{s-dc} < P_{Th}$
$V_{s-dc} > V_{Up-Th}$	"100101"	"100110"
$V_{s-dc} < V_{Lw-Th}$	"010001"	"011001"

where I_g is the current drawn from the source at the perfect match condition;

$$I_g = \left.\frac{V_g}{Z_{acc} + Z_g^*}\right|_{Z_{acc}=Z_g^*} \tag{15}$$

$$\Rightarrow \qquad I_g = \frac{V_g}{2\ \text{Real}(Z_g)} \tag{16}$$

Table I summarizes the logic behind switches changing status. This happens on the rising edge of an adjustment signal, Adj, which triggers the start of the matching. In Table I, the bit stream from Most Significant Bit (MSB) to the Least Significant Bit (LSB) shows the status of each switch in the following order "S_{LSw}, S_{LIn}, S_{MIn}, S_{MCp}, S_{RCp}, S_{RSw}".

The values for the capacitor and inductor elements are also decided by the control unit. To find a relation between inputs, i.e., measured parameters V_{env} and P_{env}, and assigned values for each element of the matching circuit, a few sample points are chosen. Based on the element values at each point and corresponding values of inputs, a linear relationship was extracted as an approximation for the relation between inputs and outputs. In addition, the element values were kept within a range that allows on-chip realization of the circuit.

More specifically, the inductance of the series inductor is determined by

$$L_{Ls} = K_{Ls}\frac{V_{Lw-Th} - V_{env}}{V_{Lw-Th}}\ , \tag{17}$$

where K_{Ls} is the coefficient determining the maximal inductance value since the fraction is always between zero and one. We note that smaller V_{env} indicates a smaller real part of the access impedance and therefore a larger inductance is needed to compensate for it.

The parallel inductor depends on the measured P_{env} via

$$L_{Lp} = K_{Lp}\frac{P_{Th} - P_{env}}{P_{Th}}\ , \tag{18}$$

where K_{Lp} sets the upper limit for the inductance. As P_{env} shows the phase matching, a smaller value of this parameter implies a greater mismatch, which should be compensated with a larger inductance.

Similarly, for the parallel capacitor we use

$$C_{Cp} = K_{Cp}\frac{V_{env} - V_{Up-Th}}{V_{Sup} - V_{Up-Th}}\ , \tag{19}$$

where in the denominator V_{Lw-Th} is subtracted from V_{Sup}, which is the power supply voltage, to limit the value of the fraction. Since V_{env} is always smaller or equal to the supply voltage, the nominator will always be smaller than the denominator. This means that the fraction will always be between one and zero and hence, the actual value of this capacitor is always between zero and K_{Cp}. Again, the larger $V_{env} - V_{Up-Th}$ the larger the mismatch and hence, the larger the capacitance needed to compensate for it.

For the series capacitor the expression is somewhat different. The reason for this is that in contrast to the other elements, its value is inversely proportional to the measured parameter, i.e., as the value of P_{env} approaches the threshold P_{Th}, less phase compensation is necessary, and since the phase of capacitor is inversely proportional to its capacitance, a larger capacitance is needed. More specifically, we use

$$C_{Cs} = K_{Cs}\frac{P_{Th}}{(K_{Limit}P_{Th}) - P_{env}} \tag{20}$$

where K_{Cs} and K_{Limit} are parameters to regulate the range of the capacitance. Specifically, $K_{Limit} = 1.05$ is applied to limit C_{Cs} if P_{env} approaches P_{Th}.

TABLE II: Parameter values used for all simulations.

Parameter	Value	Parameter	Value
K_{Cp}	300 pF	K_{Cs}	15 pF
K_{Ls}	346 nH	K_{Lp}	1.0 nH

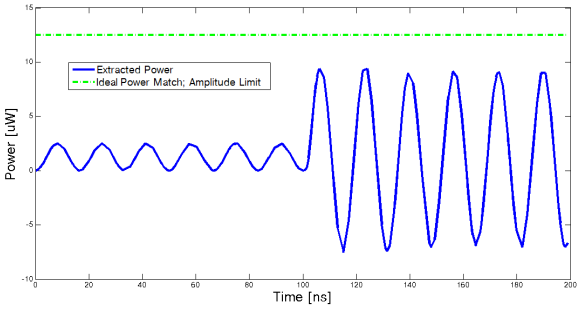

Fig. 8: Sample performance demonstration in the time domain. Transmission of power from source to the network ($Z_{acc} = 1.8\ \Omega$) before and after activating the adaptive impedance matching system at 100 ns.

III. Simulation Results and Discussion

The behavioural model for the proposed system is described using VHDL-AMS and has been simulated in Cadence using the values shown in Table II for the constants from the previous section.

A. Time-Domain Illustration

Fig. 8 shows a sample result for the power signal P_s in Eq. (3) in the time domain. In this example, the network was modelled as an impedance of $Z_{acc} = 1.8\ \Omega$. As it can be seen from the figure, when the adaptive impedance matching system has received the activation signal ($Adj = 1$) at 100 ns, it has adjusted the matching circuit so as to significantly improve the power transfer from the source into the network. With a brief glance at Fig. 8 and referring to Eq. (3) it is inferred that the matching circuit has improved both voltage-current product (the amplitude of oscillation has increased) and $\cos(\phi)$ or in the other words the phase (the mean value has increased).

B. System Performance for Different Loads and Frequencies

Based on the results of our measurement campaign reported in [13], the access impedance in VPLC systems using the frequency range from 1 to 100 MHz would cover the shaded area of the Smith chart shown in Fig. 9. The normalized real part of the impedance includes values below 5, which equals to 250 Ω (normalization was performed to 50 Ω), and the normalized imaginary part is between -3.5 and $+3.0$, which corresponds to -175 Ω and $+150$ Ω, respectively.

In order to evaluate the performance of the circuit under different scenarios, several access impedance points are chosen, which are shown in Fig. 9. As it can be seen from the Smith chart, the majority of the test points are chosen on the boundary of the impedance range, in order to test the performance in the extreme scenarios. Given the selected impedance values, the matching circuit is simulated at different frequencies.

Figure 10 shows the performance achieved with the proposed impedance matching system, in terms of the power transfer normalized to the power transferred with optimal matching. We observe that the system is able to improve the power transfer compared to the non-matched case for all network impedances for frequencies above 6 MHz. Furthermore, the value of the optimal power transfer is approached fairly closely over wide ranges of frequency, except for the very-low resistance load. In the latter case, however, very significant improvements due to impedance matching are achieved.

Fig. 11 shows the results for inductive loads. Again, notable improvements in power transfer due to matching can be observed. Furthermore, the proposed system manages to keep the power transmission within the 10% of that for ideal matching within the frequency range of about 5-50 MHz for all cases.

C. Bandwidth of the Matching Circuitry

To further investigate the characteristics of the system, in particular its bandwidth, we conducted the following experiment. The system was set to adapt its matching at the center frequencies (f_c) given in the first column of Table III. After adaptation, the adaptive matching capability was disabled and

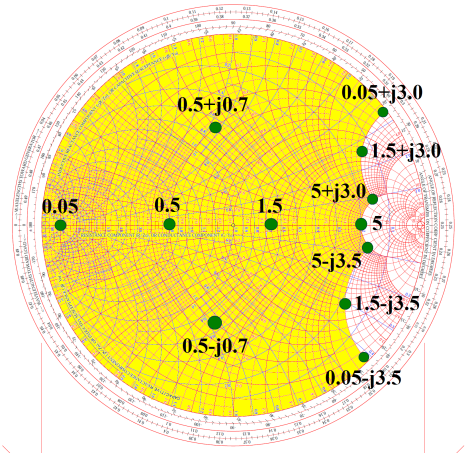

Fig. 9: Access Impedance range for VPLC applications using frequencies between 1-100 MHz [13]. The values on the chart are normalized to 50 Ω.

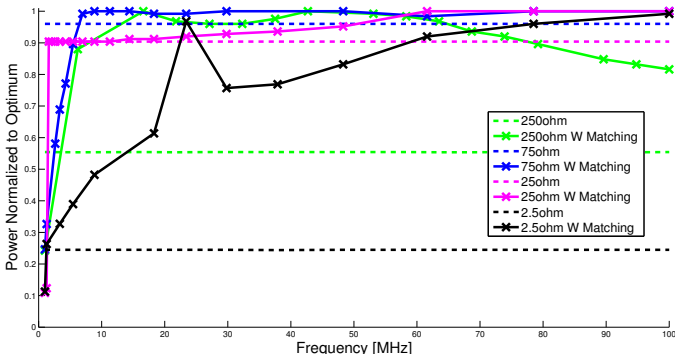

Fig. 10: Performance of the matching circuit as function of frequency for purely resistive loads.

TABLE III: Specifications for bandwidth simulations.

f_c [MHz]	Tested Band [MHz]	Access Impedance [Ω]		
		One-Tenth	Average	Maximum
80	64-96	15+j14	75+j30	150+j140
50	40-60	26+j6	40+j40	260+j60
30	24-36	10+j4.5	20+j25	100+j45
10	5-15	12.5+j6	10+j15	125+j60

the frequency of the source was altered in the frequency range shown in the second column of Table III. Furthermore, to evaluate and demonstrate the merit of the matching scheme under range of network loads, the average and maximum of the access impedance for each center frequency measured in our campaign (see [13]) was used for this test. Finally, since the real and imaginary parts of the impedance values for the measured loads are more on the larger side, also the impedance corresponding to one-tenth of the maximum access impedance was applied in the test. Table III lists the impedance values in colums 3-5.

It should be noted that since the value of loads are extracted for center frequencies (not the test band) the loads were modelled by passive elements (resistors and inductors) with a fixed value. The resistance was chosen equal to the real part of impedance in Table III and inductances were calculated by Eq. (21).

$$L_{test} = \frac{\text{Imag}(Z_{acc})}{2\pi f_c} \tag{21}$$

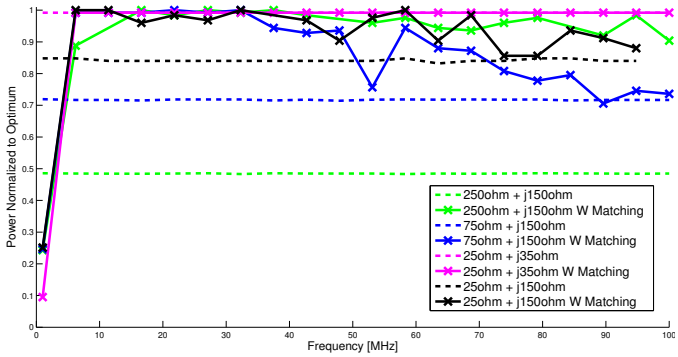

Fig. 11: Performance of the matching circuit as function of frequency for inductive loads.

Figure 12 shows the performance results, again in terms of the power transfer normalized to the power transferred with optimal matching. We observe that at middle frequencies, specially around 50 MHz, the frequency response of the matching circuit is fairly flat and shows a wideband behaviour. At 10 MHz the matching circuit shows a high-pass behaviour (better power transfer for higher frequencies). Nevertheless, for the entire band, which is equal to 100% of the center frequency, the circuit was able to improve the power transmission. At 80 MHz, the system behaves as a low-pass circuit. In some cases, specially for smaller loads, it does not manage to improve the power transmission over the entire frequency band of the test. But in this case, the power transfer is close to the optimum with and without matching. Therefore, it seems that this system with those given parameters would be suitable for wide-band usage in the mid-band as well as narrow-band. However, in lower and higher frequencies, even though improving the power transmission anyhow, it is more suitable for narrow-band usage.

D. Timings of the System

We finally make some remarks on the time that the system needs to adapt the impedance. To this end, the measurement unit settling time and the control unit decision time need to be considered.

The measurement unit needs a minimum of two cycle times ($2/f_c$) to settle, which depends to the frequency of the transmitter. That is mainly the time needed in the beginning for the rectification circuit and the capacitor in the low pass filter to get charged and represent their input value properly. However, to minimize this effect, the measurement unit is always on-line.

The decision making time of the control unit depends on both digital (mainly in Control Unit) and analog parts (mainly in Measurement Unit). The digital delay estimate is $5T_d$ where T_d is the standard delay time of the gates in corresponding circuit. The analog delay could be estimated as $3t_{rise}$, where t_{rise} is the rise time of op-amps used. However, considering 0.13 μm CMOS process as our main candidate for implementation and using its delay figures, the total delay will be less than a nanosecond. Therefore considering the maximum frequency of 100 MHz ($T_{min} = 10$ ns) for VPLC applications, this delay of less than one nanosecond will be comfortably acceptable.

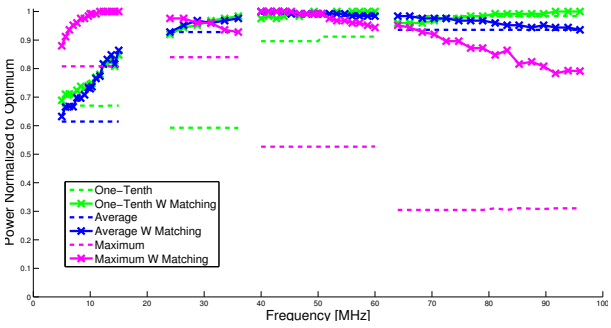

Fig. 12: Performance of the matching circuit for the four test cases specified in Table III.

It should also be mentioned that in some cases the first round of adjustment even though improving the power transmission may not necessarily be enough for the system to reach its optimal performance. However, re-evaluation of the circuit after initial matching adjustment and accordingly re-adjusting the matching circuit in those cases improves the performance. The optimal performance was always reached in lesser or equal to four rounds of adjustment.

IV. Conclusion

In this paper, we have presented an adaptive impedance matching system for VPLC. The proposed system adjusts the impedance for a given centre frequency through switching and adaptation of series and parallel inductors and capacities. The system has been described using VHDL-AMS and simulated in Cadence. The performance results have demonstrated the effectiveness of the matching system for a wide range of frequencies and network impedances.

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