On the Design of Impedance Matching Circuits for Vehicular Power Line Communication Systems

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***Abstract*—The design of power line communication (PLC) systems for vehicles, i.e., vehicular power line communication (VPLC), is a challenging task as propagation conditions are harsh and devices need to be low cost and highly integrated (to have minimal overhead on vehicle's cost and weight). One particular challenge, which is common to many PLC application scenarios, is the temporal and spatial variation of the input impedance. In this paper, we investigate on this issue and, based on previous studies and measurements on access impedances for a PLC network in a car, we discuss the design of adaptive impedance matching circuits for VPLC. This includes a study on frequency range of operation, suggestions for impedance matching circuits, and proposing a circuit structure. In particular, since inductors are an integral part of matching circuitry and given that over the typical frequency range of operation for VPLC their integration is challenging, if not impractical, we advocate the use of active inductors in matching circuits. As compared to passive inductors, they occupy a smaller on-chip size and their inductance is adjustable. We also propose an active inductor structure that provides a wide range of inductance values which are suitable for VPLC applications.**

Index Terms*—*Vehicular Power Line Communication, Adaptive Impedance Matching, Circuit Structure, Active Inductor.

I. Introduction

Power Line Communication (PLC) has been widely applied over the electricity distribution grid for, e.g., home automation and entertainment, automatic meter reading, and many other applications [1]. Recently, with the exponential growth of electronic devices in vehicles [2], this approach has also been investigated as a data communication solution in vehicles, cf. e.g. [3]–[7]. However, to communicate reliably and efficiently over power lines several challenges need to be overcome. These include frequency selectivity of the transmission channel caused by impedance mismatches in the wiring harness and impulsive noise that is introduced by electrical components connected to the harness. Another characteristic of the power line medium as a communication channel is the time and frequency selective network impedance at different access points, e.g., [1, Ch. 4], [8], [9]. Hence, impedance matching to improve the efficiency of transmission/reception of signal into/from power lines becomes an appealing concept.

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While different approaches and aspects of impedance matching have been studied in the literature, e.g., [1, Ch. 4], [10]–[15], frequency and time dependency of access impedance, which necessitate adaptive impedance matching, are often not considered or discussed in detail [8]. Therefore, in this paper different aspects of designing an adaptive impedance matching circuit for Vehicular PLC (VPLC) will be discussed.

The remainder of this paper is organized as follows. In the next section, the main approaches of impedance matching, with a focus on PLC applications, will be reviewed. Section III discusses the design of an adaptive impedance matching structure that is suitable for VPLC applications. Section IV first briefly reviews difficulties and challenges in realizing active inductors as an important part of adaptive matching circuits, and then a circuit structure for active inductors is introduced. Finally, conclusions are given in Section V.

II. An Overview of Impedance Matching

Maximizing the efficiency and power delivery via impedance matching is considered in several electrical engineering disciplines including power systems, amplifier design, and antenna and filter design. In this section, we first briefly review impedance matching concepts and methodologies. Then, a more detailed study on impedance matching for PLC and its application to VPLC are presented.

A. General Impedance Matching

A power source is able to deliver its maximum power only if the impedance seen at its ports is the complex conjugate of its internal output impedance. A similar statement holds for a load to be able to receive the maximum power through its ports. However, often this complex conjugate matching is not the case. Hence, to maximize efficiency of power delivery an impedance matching circuit is needed to transfer the access impedance to a matched impedance at the ports of transmitter or receiver. This is illustrated in Fig. 1. To design the impedance matching circuit without power loss, circuits based on lossless passive elements (either lumped elements such as inductors and capacitors or distributed elements such as transmission lines) are among the most popular impedance matching solutions, cf. e.g. [15], [16, Ch. 5], [17].

Impedance matching solutions can be classified into different categories based on the design criteria.

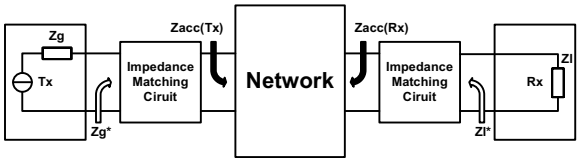


Fig. 1: Connection of a transmitter and receiver to a two port network via impedance matching blocks.

- Considering the design methodology of impedance matching circuits, two classes of methods, namely, analytical methods, which use an approximate circuit model for the load (in the case of PLC, both load and network), and numerical methods such as real frequency technique, rational parametric approximation, and direct stochastic approximation [13] can be distinguished [15].
- In the terms of load/source characteristics, impedance matching problems can be divided into three classes [18]. First, the filter or insertion loss problem, in which matching a resistive load to a resistive source is considered. Second, the single matching problem, where a resistive source is to be matched with a complex load. And third, the double matching problem, in which both load and source have complex impedances.
- From the implementation point of view, the impedance matching system design can be classified into two categories: flexible or fixed structures. In the former, circuit topology is optimized together with the values of the components. For the latter, only the values of components can be chosen to obtain the best match possible. Therefore, some design goals may be compromised in favour of simplicity of the structure.
- In terms of frequency range of operation, matching circuits can be narrowband or wideband. In some cases, wideband matching is achieved via several narrowband matching schemes, e.g., [19].

Another aspect when implementing impedance matching is the use of lumped elements or transmission lines. However, due to the low frequency range ($\leq$ 100 MHz) of typical VPLC applications, a transmission-line-based implementation is usually not practical due to the large size of such lines [16, Ch. 5]. When using lumped elements, off-chip components such as transformers are not favourable due to the size, cost and space constrains. Furthermore, all of the above approaches can be considered for a constant or varying impedance, the latter calling for an adaptive impedance matching network.

B. Impedance Matching in PLC

We now overview impedance matching systems, particularly those proposed for PLC applications, and discuss their advantages and disadvantages, especially, in the context of their use for VPLC.

1) Phase and magnitude screening and capacitor bank adaptive impedance matching: In [10], the authors describe a PLC system that performs impedance detection via reading the phase and magnitude deviation from a reference impedance,

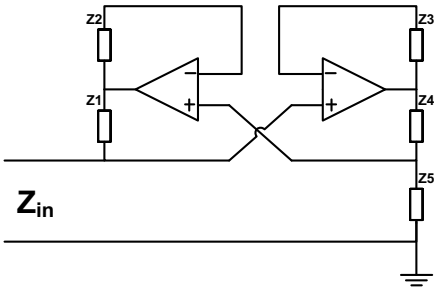


Fig. 2: VCGIC used in [8] to provide necessary variable inductor for matching circuit.

e.g. 50 or 100 Ω. Impedance matching is accomplished via a fixed inductor combined with a capacitor bank controlled by semiconductor switches. To decrease the range of impedances to be matched they also suggest an optional use of a transformer. The design is based on an analytical method and a fixed L-structure, and impedances ranging from a few Ω to few MΩ can be matched. However, matching is limited to a very narrow band.

2) Optimizing transformer winding ratio: In [1, Ch. 4], van Rensburg discusses different aspects of coupling to the power grid. The emphasize is on transformers, specifically when it comes to an attempt of matching impedances. Optimizing the winding ratio of transformer and using different taps are the main suggestion which are studied in details, implemented and tested.
The major disadvantage here is the price and size of transformers which directs the interests toward using transformer-less solutions [20].

3) PLC Impedance Adaptation using VCGIC: In [8], Park et al. comment on previous work for adaptive impedance matching and point out that many external (i.e., off-chip) components such as capacitors, switches and transformers increase the price and size of matching circuits. To address these problems, they suggest the use of a Voltage Controlled General Impedance Converter (VCGIC), as proposed in [21] and shown in Fig. 2.

The impedance seen at the input of this circuit is given by

$$Z_{GIC} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \,, \tag{1}$$

and thus different impedances can be adjusted depending on the chosen values for Z_i, $i = 1, \ldots, 5$. For example, choosing Z_2 as a capacitor and the other elements as resistors, the equivalent impedance will be an inductor. This provides an extended flexibility to this system and makes it more suitable with Integrated Circuit (IC) technology by avoiding the use of inductors. The maximum current and voltage supported by operational amplifiers impose some limits on this circuit. This is overcome with the addition of a fixed inductor and a transformer in [8], which has the disadvantages of additional cost and size.

The methodology used in [8] is based on an analytical circuit model to solve a single-matching problem via sensing the peak current through a transformer [12]. The implementation

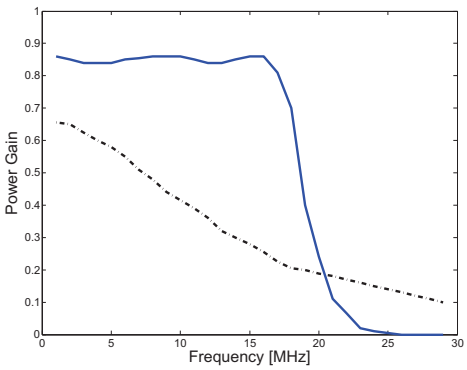


Fig. 3: Power transfer gain between modem and power line network with (blue solid line) and without (black dashed line) wideband equalizer. Results taken from [13, Fig. 5]

is with a fixed structure and achieves narrowband matching within the range of $[6.4, 25]\ \Omega + \mathrm{j}2\pi f [7.5, 24]\ \mu\mathrm{H}$.

4) Impedance Adaptation using Fuzzy Logic: A series LC circuit and a transformer are used in [11] as adaptation circuit. The off-chip variable inductor and transformer are controlled by a digital circuitry in order to match the phase and magnitude of the access impedance in an automatic fashion. The decision making process chosen in this study is based on a fuzzy logic algorithm which, compared to other numerical approaches discussed below, seems to have a lower computational complexity. Disadvantages are the use of discrete variable transformer and inductor as part of the circuit and the need for a digital control system.

5) PLC Wideband Equalizer: Araneo et al. [13] present a study on wideband impedance matching, using a numerical approach, namely a vector fitting method. They suggest using a Meta-Particle Swarm Optimization (M-PSO) algorithm for calculations and compare it with some other methods such as genetic algorithms. Their study shows that M-PSO is able to converge to the solution after approximately one thousand iterations. The solution devised for this single-matching problem is to find the zeros and poles of an LC-ladder structure to enable the maximum power transmission. The coupling circuit for this wideband matching is referred to as equalizer, as it does not necessarily match the impedance throughout the band but rather increases the power transmission toward maximum. As shown in Fig 3 (taken from [13]), the power transfer gain between modem and network is less than 1 over the frequency range of interest, i.e., the network impedance is never matched at any point in the frequency band of interest.

In a similar work by Issa et al. [14], a recursive algorithm called Weinberg relations is developed and a Tchebycheff gain function has been used as the equalizer structure. The matching behaviour of their proposed system is also similar to what is seen in Fig. 3.

We note that the use of numerical optimization methods requires a digital processor, which may be considered a disadvantage when aiming for small-area integrated solutions.

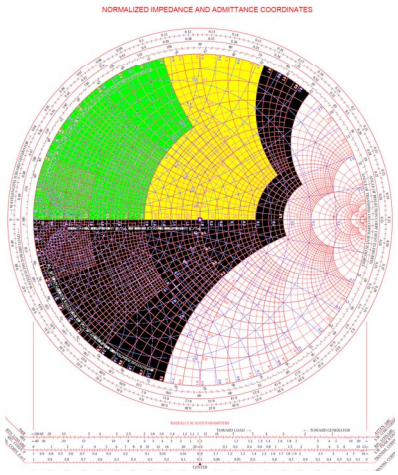


Fig. 4: Smith chart illustration of access impedance range according to measurement results from [9]. Coloured areas: access impedance range to be covered for matching, frequency range 0 to 100 MHz. Yellow and green areas: reduced range when excluding some measurements, frequency range 0 to 100 MHz. Green area: reduced range and frequency range 0 to 40 MHz.

III. On the Design of an Adaptive Impedance Matching for VPLC

Having reviewed various impedance matching approaches in general and for PLC in particular, we now move on to VPLC. Based on the results from a measurement campaign presented in [9], we discuss different aspects of an impedance matching circuit and then present an adaptive impedance matching circuit structure.

A. Frequency Range and Bandwidth

Figure 4 shows the measured access impedance ranges for a combustion-engine car (Pontiac Solstice) from [9] on a Smith chart. The total coloured area (black, yellow, and green) shows the region of the Smith chart that should be handled by an impedance matching circuit. This region is applicable for the frequency range from ≈0 MHz to 100 MHz. Proper matching for the entire area requires a complex matching circuit structure and passive components with large values. Furthermore, adaptive matching requires a flexible control scheme for adaptation. Ignoring outlier access impedances in the data from [9] the target area reduces to the yellow and green shaded parts in Fig. 4. Furthermore, if we limit the upper frequency bound of the target band to 40 MHz, then only the green area in the Smith chart needs to be covered. These considerations, which need to be studied further for other vehicles as well as different vehicle types, indicates the trade-off between frequency range and complexity of the matching circuit.

Another interesting result from [9] is the effect of existing relays in the vehicle power line network at low and high frequencies. At low frequencies, when certain relays are open, they disconnect certain power line path and hence disable communication between these nodes. However, due to the parasitic capacitance of these relays, above a certain frequency they behave as a short circuit regardless of their status (open or close). Furthermore, the battery and loads considered in

[9] exhibit low impedances at low frequencies, which makes matching a more challenging procedure. Hence, choosing the lower frequency bound in the MHz range seems to be a reasonable choice. This is consistent with the frequency ranges considered in most studies as well as products for VPLC, cf. [9, Fig. 1] and [22].

When considering the bandwidth for impedance matching, it should be noted that measurement campaigns have shown highly frequency-selective VPLC transfer function [6], which is a result of the many signal reflections at unmatched branch points and loads. This property adds significant challenges to an already complex procedure of common wideband matching. That is, in wideband matching usually the equalizer is a circuit which compensates the rather smooth downward slope of system to a flat transfer function, see e.g. in Fig. 3. In the context of network impedances in VPLC with abrupt changes over frequency, wideband matching using several narrowband matching circuit such as in [19] is a promising approach. Therefore, in the following we consider narrowband matching.

B. Methodology and Circuit Structure

For adaptive impedance matching both an analytical or a numerical approach can be applied. The latter requires notable computational effort, while the former can tune component values based on phase and magnitude of the access impedance with less complexity. Pursuing the analytical method, which is more suited for low-cost and integrated VPLC solutions, the choice of proper structure should be made. Fixed structures used in previous works may overly restrict the matching ability or require wide tunability range for its components. A completely flexible structure which can be adapted online is not realistic either. Therefore, we suggest a structure with some flexibility such that the expected range of impedances, as illustrated in Fig. 4, can be covered.

The Smith chart can be used as a graphical tool for matching the load to the desired impedance. On the Smith chart, each impedance is represented by a point. Thus the task of matching breaks down to finding a path between the location of the load and the location of desired impedance on the Smith chart. Without loss of generality we assume this impedance at the center of the Smith Chart, 50 Ω, which is the typical internal resistance of signal generators. Considering the aforementioned single-matching problem, since the centre of Smith chart represents 50 Ω, the matching problem is to find a path between the load point and the centre of Smith chart. Since lossless matching is desired, this path should be found through contours of constant reactance or susceptance on the Z-Smith chart and Y-Smith chart (red and blue curves in Fig. 4).

Using the expected range of VPLC access impedances according to the results from [9], the circuit structure shown in Fig. 5 is extracted from Fig. 4. By proper arrangement of switches, this circuit can adjust its configuration to behave as a T-structure or two different L-structures. For the range of values for each element of the circuit we obtain the following results (all the capacitances are in Farad and inductance are in Henry, and f is the frequency in Hertz):

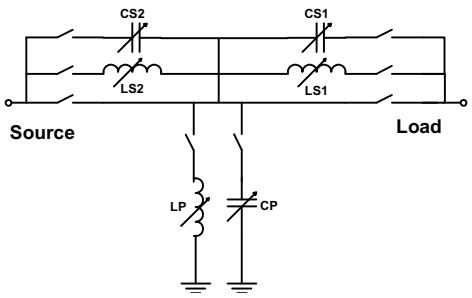


Fig. 5: Structure of adaptive matching circuit according to the VPLC access impedance range in Fig. 4.

$$\frac{6.37\times10^{-6}}{f} < \text{CSL} < \frac{637\times10^{-6}}{f} \tag{2}$$

$$\text{LS} < \frac{3.978}{f} \tag{3}$$

$$\text{CP} < \frac{7.957}{f} \tag{4}$$

$$\frac{6.37\times10^{-3}}{f} < \text{LP} < \frac{63.7\times10^{-3}}{f} \tag{5}$$

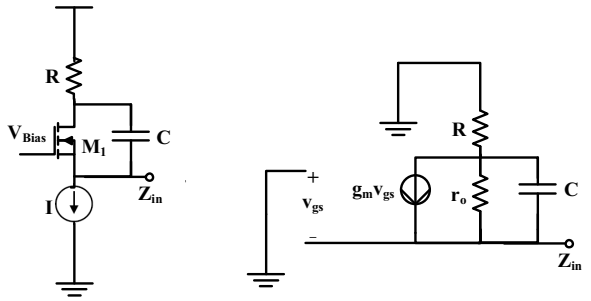
$$\frac{6.37\times10^{-6}}{f} < \text{CSS} < \frac{31.8\times10^{-3}}{f}\,. \tag{6}$$

By controlling the configuration of the circuit and tuning the values of its components, the network can adaptively match the impedance range shaded yellow and green in Fig. 4 (i.e., the relevant range when neglecting outliers) to 50 Ω.

IV. An Active Inductor Structure

As mentioned in Section II-B, inductors are one of the main components of impedance matching circuits. However, given the frequency range of interest, lumped passive inductors are bulky and expensive elements and their integration on an integrated circuit (IC) platform is impractical [8], [17], [23], [24]. The larger the value of the inductance and the lower the frequency, the bulkier the lumped element and the more difficult its implementation in an IC [24]. Therefore, for various applications such as RF filters and oscillators, active circuits are used to mimic the behaviour of inductors [24]. The above-mentioned VCGIC circuit presented in [8] is an example for this approach being used in PLC impedance matching.

Even though the VCGIC-based implementation requires a chip area that is smaller than a passive inductor, it still requires a relatively large number of transistors and thus chip area. Another popular and less complex approach to implement active inductors is to use two gyrators [24]. Since the simplest gyrator is a single transistor amplifier, an active inductor core circuit can consist of a minimum of two single-transistor amplifiers. As noted in [25], single-transistor amplifiers, in particular, output impedance of a common-drain buffer (source follower), can mimic inductive behaviour. In this section, we propose an alternative active inductor structure that is also based on a single-transistor amplifier, namely a common-gate amplifier. This structure is simple, occupies a small chip area, and is capable of providing high inductance values at low



(a) Schematic (b) Equivalent small signal model

Fig. 6: Proposed active inductor circuit.

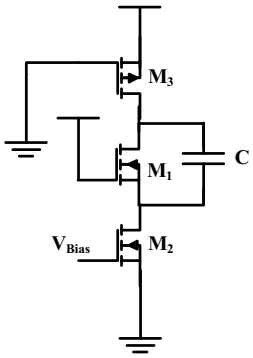


Fig. 7: Schematic of the simulated active inductor

frequencies. To confirm the validity of the structure, the circuit is designed and simulated in a 0.13 μm CMOS technology.

A. Circuit Structure and Functionality

The proposed circuit and its simplified small-signal model are shown in Fig. 6. The input impedance of this circuit shows an inductive behaviour which can be modelled by an ideal inductor with series and parallel parasitic resistances. There is also a parallel parasitic capacitance, however, its value is low and thus over the frequency range of interest it can be neglected. From the analysis of the model shown in Fig. 6(b), the values of the equivalent elements can be obtained as:

$$L = \frac{C}{G(g_m - G)} \quad (7)$$

$$R_s = \frac{G_o + G}{G(g_m - G)} \quad (8)$$

$$R_p = \frac{1}{G}, \quad (9)$$

where G is the equivalent conductance of resistor R, C is the capacitor connected between drain and source of transistor M1, and g_m and G_o are the transconductance and the output conductance of the transistor. As it can be seen, the value of inductance can be changed not only by changing the bias current, i.e., g_m, or load conductance, i.e., G, but also by changing the value of the added capacitor, i.e., C. By properly tuning these parameters a wide range of inductance values can be achieved. Note that by changing the bias current the power consumption of the circuit also changes. The tunability and high level of integration come at the cost of an additional power. Note that passive inductors ideally do not dissipate power, however, at low frequencies, they are bulky and typically are not tuneable. As shown in the next section, the power overhead of the proposed structure is on the order of few μW to a few tens of μW and depending on the application it can be optimized.

B. Simulation Results

To evaluate the proposed structure, several sample active inductors based on the circuit shown in Fig. 7 are simulated in a 0.13 μm CMOS technology. Note that in this circuit, instead of the load resistor, a transistor biased in triode is used. As mentioned above, the circuit is capable of providing a wide range of inductance over the frequency range of interest with inductance values from μH to few mH and beyond. Fig. 8 shows the simulation results for the equivalent inductance and equivalent series resistance of a sample circuit of the proposed structure. Inductance has been varied by changing the capacitance C, from 500 fF to 5 pF (by switching in or out capacitors in a capacitor bank). The overall power consumption for this particular circuit is less than 2.6 μW. Note that changing the capacitance (C) does not affect the power consumption.

As it can be seen from the Fig. 8 this structure can cover a wide range of inductances (from μH to mH), however, it has a relatively high series resistance. To reduce the series resistance, a negative resistance structure, namely, a standard architecture based on cross-coupled transistors [25], has been added. Although the inclusion of the aforementioned negative resistor reduces the equivalent series resistance, this amendment comes at the cost of increased power consumption (93 μW power overhead) and decreased inductance. This effect is illustrated in Fig. 9 where we show simulation results obtained after adding the negative resistance structure. In this case, the

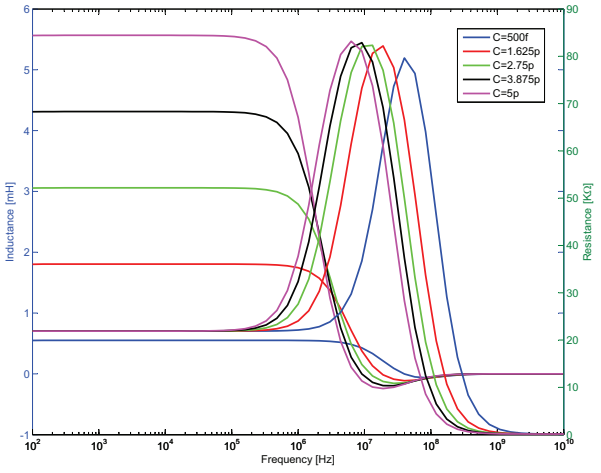


Fig. 8: Proposed active inductor; Effect of the capacitance C on the equivalent inductance and series resistance.

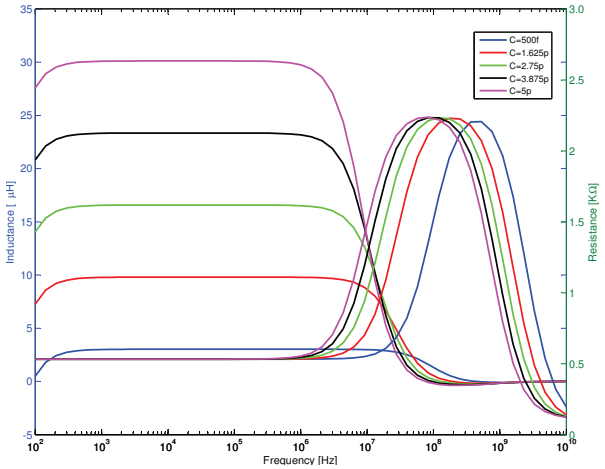


Fig. 9: Proposed active inductor with additional negative resistance; Effect of the capacitance C on the equivalent inductance and series resistance.

capacitance C was changed from 1 pF to 10 pF.

V. Conclusions

Considering the growth in the number of electronic components in vehicles and with it the increasing complexity, cost, and weight of the wiring harness, PLC is a promising approach for data communication in vehicles. One of the main challenges for VPLC is the coupling loss due to impedance mismatch. In this paper, we have reviewed the concept of impedance matching providing general classifications and discussing impedance matching solutions presented for PLC. Using results from previous measurements on a combustion-engine car, we have presented an structure for an impedance matching circuit, which is flexible enough to meet the target impedance ranges. Furthermore, since one of the important components needed for impedance matching is an inductor, which requires a large on-chip area if integrated on a chip, an active inductor structure is proposed and its performance is validated through circuit-level simulations in a 0.13 μm CMOS technology. Future work will extend the considerations to measurements of access impedances of several vehicles and the design of an integrated coupler that includes an adaptive impedance matching circuit.

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