A NEW HIGH SPEED, LOW POWER ADDER; USING HYBRID ANALOG-DIGITAL CIRCUITS

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***Abstract*—In this paper a new high speed and low power adder is presented. The circuit uses a hybrid concept of analog and digital circuit design to propagate the carry and so achieve a Full Adder with 78^{ps} delay and $7.26^{\mu w}$ of power consumption. SPICE Simulations performed on the $0.18^{\mu m}$ TSMC Technology demonstrates the average improvement of 159%, 184% and 516%, respectively for Delay, Power Consumption and PDP.**

***Index Terms*—High Speed, Low Power, Hybrid Analog-Digital Circuit Design, Full Adder.**

I. INTRODUCTION

ADDERS are the most basic parts of almost every digital circuit and they strongly affect the overall performance of processors [1, 2]. Nowadays, circuits with low power and high speed have a great importance. Specially regarding to development of mobile systems such as portable computers and cell phones, many researches are dedicated to high speed, low power circuits [3, 4, 6]. Consequently, as a critical part of digital processors, adders are largely studied [3-6].

Whereas analog circuits consume very low amount of power and have a high speed [7], for some problems such as a long time design procedure [8] they were not developed as processor, in contrast with digital counterparts. However, recently, designers used both concepts of analog and digital circuit design to achieve hybrid processors with positive properties of both analog and digital circuits [9-13]. In this paper also we've used hybrid analog-digital circuits to make and adder with better properties (i.e. with reduced delay and power consumption).

Fig. 1. demonstrates general structure of a full adder; consisting of two half adders and an OR gate. Regardless of implementation details of half adders, they've to include at least one gate. With a supposed minimum delay time of *t* for the gates, simply critical path (the path with maximum delay which determines the overall delay of full adder) can be recognized; it's "carry out" path with *3t* delay (shown in Fig.1).

It is also obvious that the minimum of supposed unit time, *t*, might be the transition delay of a transistor for changing the operation mode. Therefore digital full adders will have a valid output at least after three transistor delay time. It is exactly the point where this paper will focus on. It is tried to decrease this delay which in turn will decrease the overall delay time of the Full Adder. To figure out mentioned discussions, a conventional transistor level realization of a CMOS full adder has been inserted in Fig. 2.

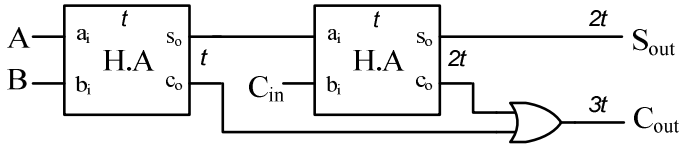

Fig. 1. General Structure of a Full Adder and Delay Propagation.

It is noteworthy that also in an *n*-bit adder consisting of *n* full adders, again the carry propagation path is the critical one and determines the overall delay (Note Fig. 3) . Names of different adders (Carry Save Adder, Carry Look ahead and so forth) in the literature [1, 14] witnesses the importance of carry propagation and the amount of works dedicated to.

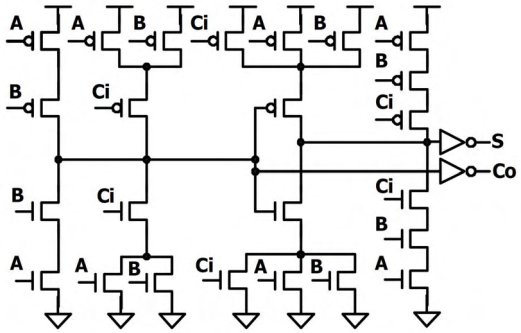

Fig. 2. A Conventional Transistor Level Realization of a Full Adder [14].

This paper is organized as follow; In the next section the new proposed hybrid analog-digital adder will be presented. The third section is dedicated to simulation, while the fourth one includes discussion and comparisons. Finally, the fifth section concludes the paper.

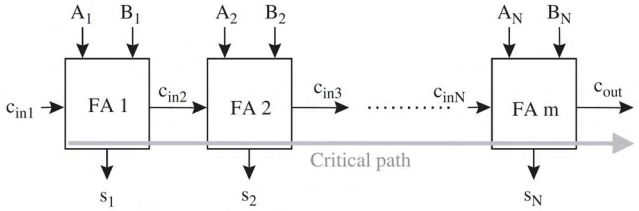

Fig. 3. Critical Path Delay; Carry Propagation is very deterministic [15].

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II. Proposed Hybrid Analog-Digital Circuit

A. Carry Propagation

As mentioned before the carry propagation path is the critical one, either in a single full adder and in an *n*-bit adder. Through this path at least three transistors exist which should change their mode from cut-off to saturation and/or vice-versa. This is the innovation bearing point; where the new hybrid analog-digital circuit omits an obligatory stage of digital circuits. Proposed circuit is seen in Fig. 4 and as it is conspicuous, the circuit encompasses only two stages.

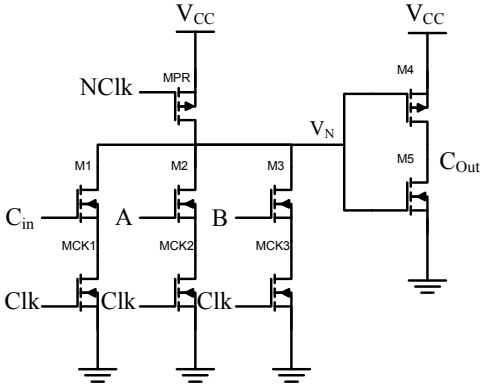


Fig. 4. Proposed Hybrid Analog-Digital Carry Propagation Circuit.

First Stage (i.e. Input stage), consists three transistors aligned to three inputs of a full adder and the second stage includes two transistors, producing the output. However, the functionality is as follow:

Node *N* is pre-charged to V_{CC} by *MPR* at *NClk* period. At *Clk* period, transistors which have a high input, can discharge the mentioned node. As the node *N* has a capacitance, the voltage variation of the mentioned node is related with the drawn current as (1);

$$\Delta V_A = \frac{I}{C}\Delta t \tag{1}$$

So with different current values, corresponding to different situations of input (the numbers of saturated transistors which have high inputs), the voltage variation of node is different. This produces four different levels of voltage for node *N* (as it's seen in Table I).

TABLE I
INPUT-OUTPUT TABLE OF CARRY PROPAGATION CIRCUIT

# of High Inputs	Voltage Level*	Output Situation**
0	Highest	Low (0)
1	High	Low (0)
2	Low	High (1)
3	Lowest	High (1)

* Qualitive Expression of Voltage Levels
** Digital Voltage Levels

Cofiguring the *W* to *L* ratio of two right-most transistors of Fig. 4, the trigger level can be assigned to the correct voltage level of node N (i.e. between High and Low in Table I) to provide a true output. Table I consists Input-Output relation of proposed hybrid analog-digital carry propagation circuit.

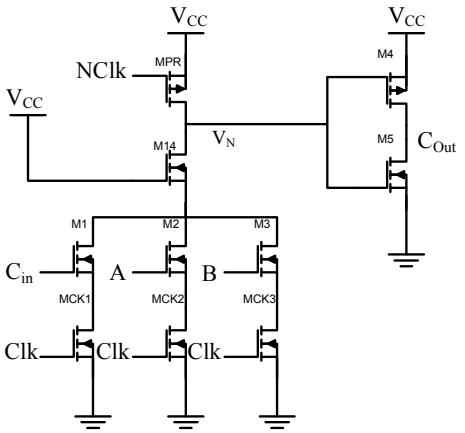
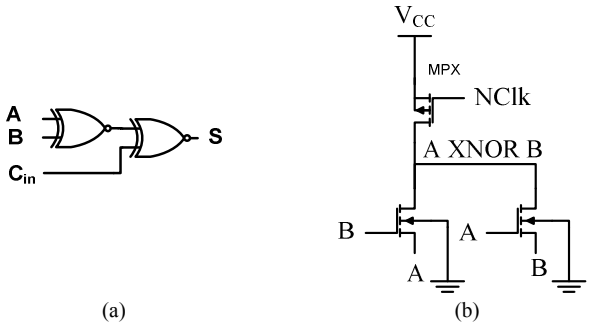


Fig. 5. Final Hybrid Carry Propagation Circuit.

However, some parameters such as clock time variation, size of transistors and capacitance couplings may affect the voltage of node *N*. While normal and reasonable variation of clock time and size of transistors may move the absolute value of voltage levels, regarding to large distance of different voltage levels of node *N*, they don't affect overall functionality of circuit. In contrast, capacitance coupling of inputs with node *N* (which may occur in large amounts), may have destructive effects and so to prevent it another transistor (*M14*) is added to circuit, resulting the final circuit inserted in Fig. 5.

B. Summation

For summation a simple digital circuit consisting of two XNOR gates has been used to produce output summation as in Fig. 6-(a).



(a) (b)

Fig. 6. (a) Digital Circuit for Summation, (b) XNOR circuits used in part (a).

XNORs of Fig. 6-(a) are implemented by circuit shown in Fig. 6-(b). When both inputs are high, or low, both transistors would be in cut-off and so the output remains at high level which was pre-charged to. If one of inputs are high and the other is low, then one of the transistors (which has a gate node at high level and source at low level) will be in saturation and discharges the output node. Therefore the final circuit of summation was implemented as demonstrated in Fig. 7.

III. Simulation

To study performance of the proposed circuit, it was simulated on SPICE, with the $0.18^{\mu m}$ TSMC Mixed-Signal SALICIDE technology file. Process parameters are inserted in Table II.

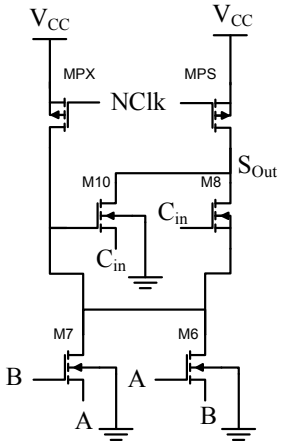


Fig. 7. Final Summation Circuit.

As one of the properties of used technology, the minimum width and length of transistor are $0.22^{\mu m}$ and $0.18^{\mu m}$, respectively. Therefore to minimize the die area, default size of all transistors were supposed to be 0.22/0.18 instead of 1 (which had to be 0.22/0.22). Transistors with different sizing are mentioned in Table III.

TABLE II
PROCESS PARAMETERS OF USED TECHNOLOGY FILE FOR SIMULATION.

Parameter	Value	Units
Min. Feature Size	0.18	µm
C_{ox}	86.8	$\mu F/\mu m^2$
$\mu_{n0}C_{ox}$	3.81	$\mu A/V^2$
$\mu_{p0}C_{ox}$	0.85	$\mu A/V^2$
W_{min}	0.22	µm
L_{min}	0.18	µm
V_{Tn0}	0.47	V
V_{Tp0}	-0.45	V
V_{DD}	1.8	V

The supply voltage is 1.8^{V} and so the rail was divided in three regions of Logical Low ($0\text{-}0.6^{V}$), Meaningless ($0.6\text{-}1.2^{V}$) and Logical High ($1.2\text{-}1.8^{V}$) which leads to the best noise margin as well

TABLE III
TRANSISTORS WITH SIZES OTHER THAN 0.22/0.18

Transistor	W [µm]	L [µm]
MPR	0.66	0.18
M 4	0.88	0.18
M 5	0.22	0.22
M 14	3.3	0.22

The results of simulations are shown in Fig. 8. They demonstrate that the maximum delay for the carry to be prepared for next stage is 78^{ps} while the average power consumption for each bit is $7.26^{\mu W}$.

IV. DISCUSSION

To have a better comprehension about the achieved results, they were compared with four recent papers. Graphic comparisons of Delay and Power Consumption are illustrated in Fig. 9 and Fig. 10, respectively.

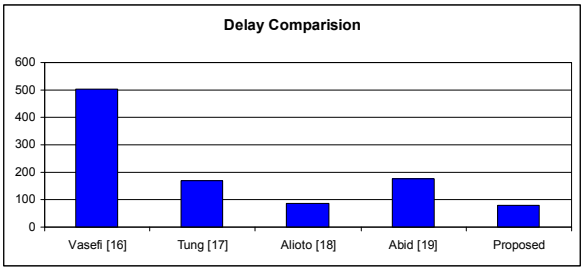


Fig. 9. Delay Comparison of Different Recent Works.

It should be mentioned again that as discussed before, the carry propagation delay is determinant in overall delay and so delay comparisons have been made among carry propagation delays.

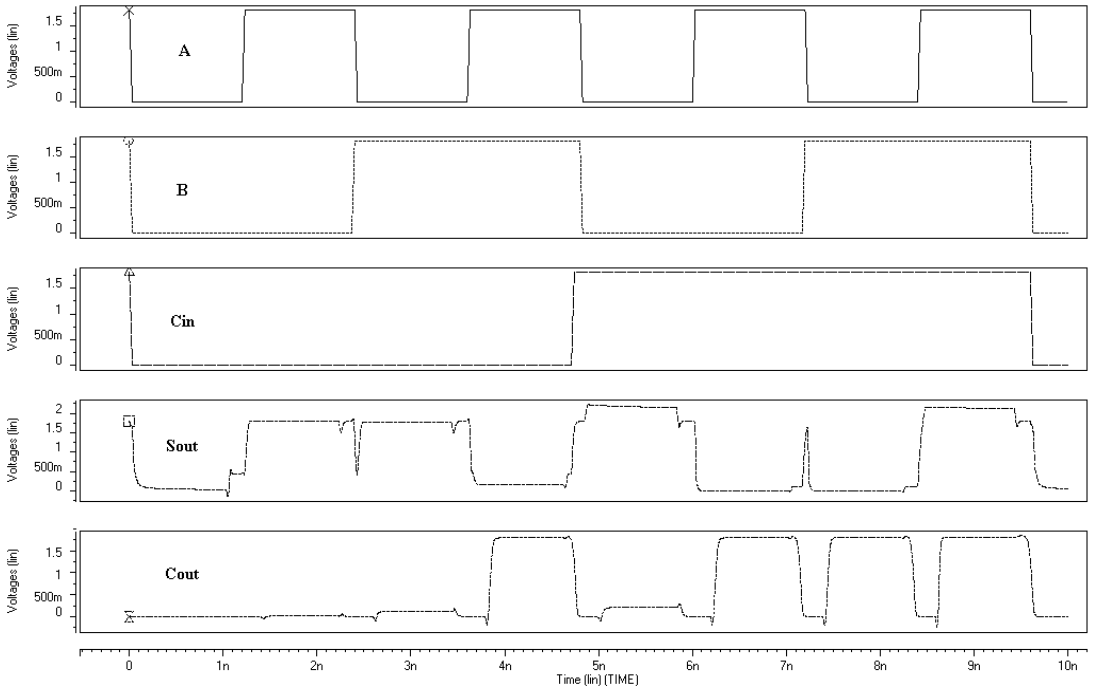


Fig. 8. Simulation results for different inputs of the proposed Full Adder.

It's conspicuous that except the proposed circuit, there is only one work with less than 100^{ps} delay and in comparison to that work we had almost 9 percent of improvement.

On power consumption also there is merely one other work with less than $10^{\mu W}$ of power consumption. This time, that circuit has be less power consumption even than proposed circuit, but it should be noted that solitary comparison of power is not truly demonstrative of a circuit eligibility. Actually, the best criterion for comparison is Power Delay Product (PDP). Considering PDP criteria, the proposed circuit is extremely better than FA proposed in [16], which has a better power consumption than new proposed circuit. By the way, to have a better view of different aspects of proposed circuit and other works, numerical results, comparisons and improvements are inserted in Table IV.

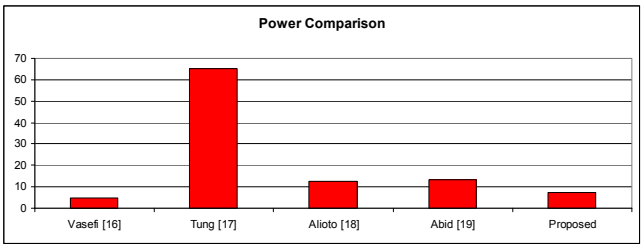


Fig. 10. Power Comparison of Different Recent Works.

It can be easily seen that in all cases new proposed hybrid analog-digital circuit could improve predecessor full adders in delay, power consumption and PDP criteria. The only exception is the power consumption respecting to that one proposed in [16], in which the power consumption of proposed circuit was 33.7% worse than [16] while the delay has been 544% improved. Hence, the accomplished speed compensates the lost in power consumption and referring to PDP criteria, again a 326% improvement has been gained. However, the average improvement is 159% in Carry Propagation Delay and 184% in Power Consumption. Eventually, the PDP was improved by a 516%. The improvements witness the eligibility of new proposed hybrid analog-digital adder.

TABLE IV
ANALYTICAL COMPARISONS OF PROPOSED CIRCUIT WITH OTHER WORKS.

	Delay	Imp. %	Power	Imp. %	PDP	Imp. %
Vasefi [16]	502	544	4.81	-33.7	2.41	326.4
Tung [17]	170	118	65.2	798	11.1	1857
Alioto [18]	85.2	9.23	12.67	74.5	1.08	90.63
Abid [19]	175	124	13.16	81.3	2.30	306.7
Proposed	78	-	7.26	-	0.57	-

* Delays are inserted in ps,.and Powers are inserted in μW.
*** PDPs are inserted in 10^{-21}×J.

V. CONCLUSION

In this paper a new adder circuit was proposed which benefits the privileges of both analog and digital circuits and so it is called Hybrid Analog-Digital.

Proposed circuit has a very low delay and power consumption and therefore an extremely improved Power Delay Product (PDP). This new high speed Full Adder could achieve a 78^{ps} delay per bit which means an average of 159% improvement, regarding to other comparable works. It also consumes $7.26^{\mu W}$ of power which is equal to 184% improvement, comparing to other works. Finally, notable improvement of 516% is achieved by a 5.7×10^{-22} J PDP.

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